

Model Name: GA-H110M-DS2

rev:1.0

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1151-A
05	CPU_LGA1151-B-DDR4
06	CPU_LGA1151-C
07	CPU_LGA1150-D
08	DDR4 CHANNEL A
09	DDR4 CHANNEL B
10	PCH_CLK BUFFER
11	PCH_DMI,USB,PCIE
12	PCH_MISC
13	PCH SATA,PCIE,SATA_EXPRESS
14	PCH_PWR,GND
15	Dual BIOS
16	ITE 8628 LPC IO
17	HWM
18	FAN CTRL--SIO
19	PCI EXPRESS*16 SLOT
20	PCI EXPRESS*1 SLOT
21	SATA
22	ISL95858_856 PWM
23	ISL95858_856 MOS_VCORE
24	ISL95858_856 MOS_VCCGT
25	VCCSA_VCCIO_VCCPLL
26	RT8237_DDR_VDDQ
27	RT8068_VPP

SHEET

TITLE

28	RT8237_PCH_VCC1_0_PCH
29	DISCRETE POWER
30	ATX POWER , A_-PROCHOT
31	KB_MS_USB
32	RTD2168 - DP to VGA - IC
33	RTD2168 - DP to VGA - Conn
34	R_USB30
35	REALTEK - RTL8111G
36	USB20_LAN CONNECTOR-RTL8111G
37	Realtek ALC887
38	REAR AUDIO JACK
39	F_USB30
40	F_USB20
41	COM , LPT , TPM
42	F_PANEL
43	EMI/ESD
44	POWER MAP
45	TABLE LIST
46	NTC MAP
47	
48	
49	
50	
51	

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Title		
Cover Sheet		
Size	Document Number	Rev
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Model Name: GA-H110M-DS2

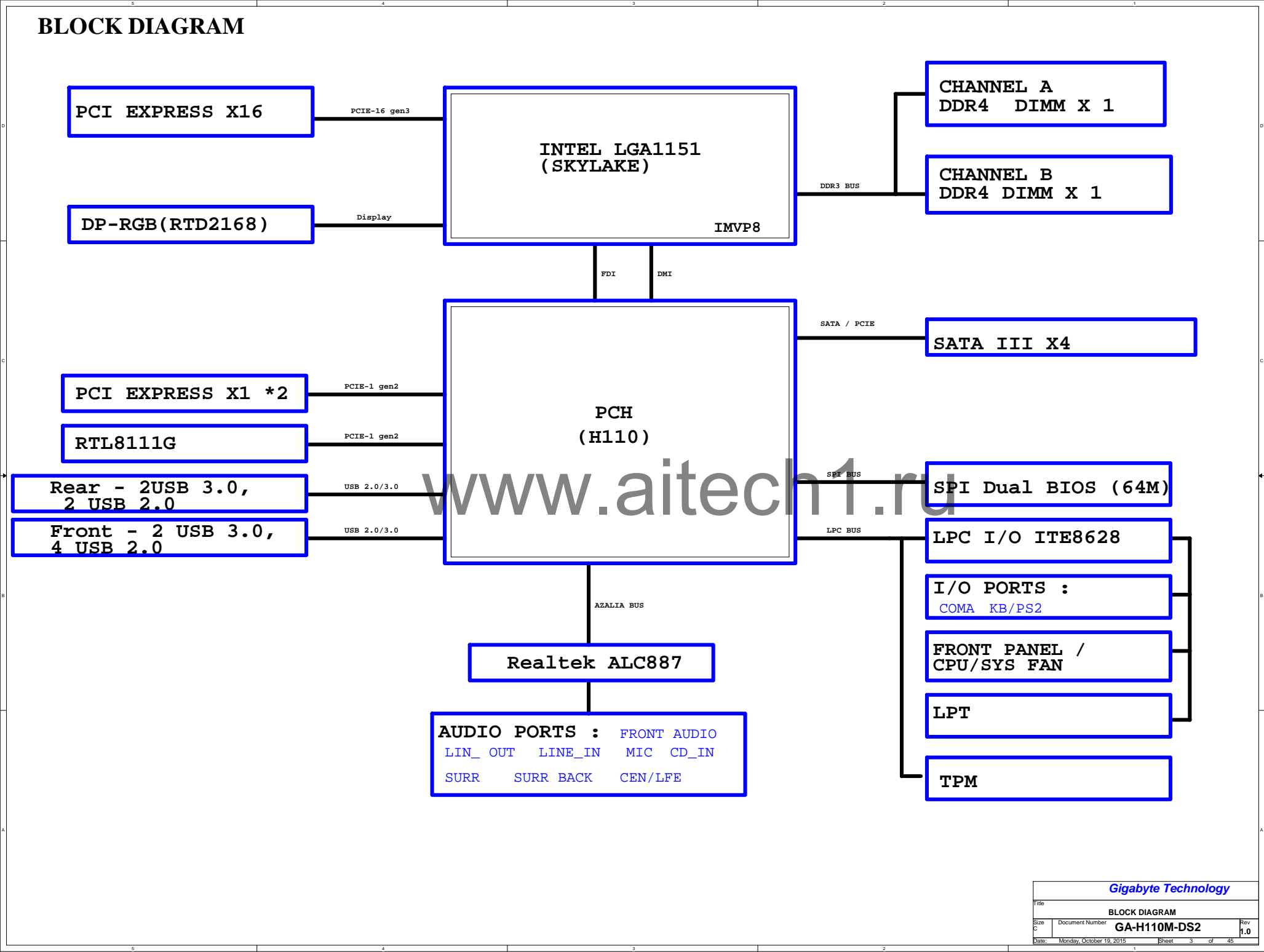
rev:1.0 Circuit or PCB layout change

Component value change history

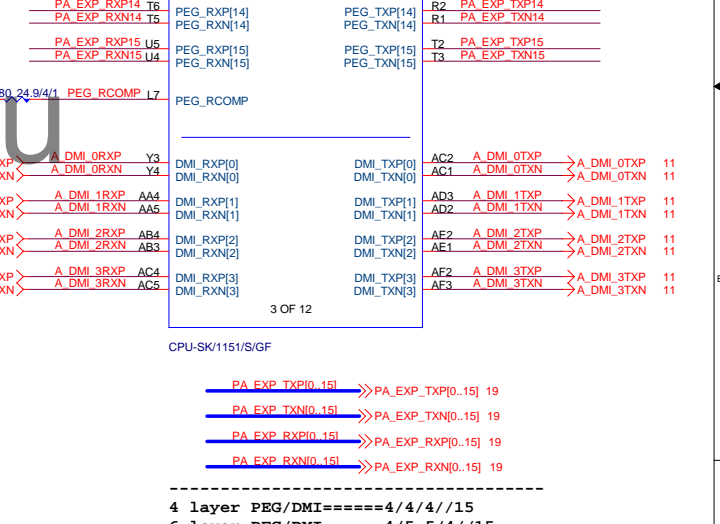
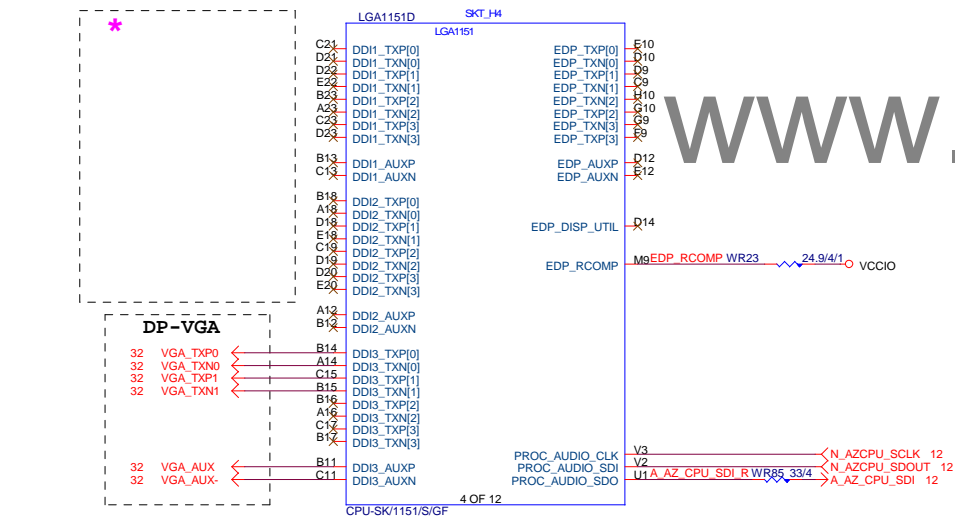
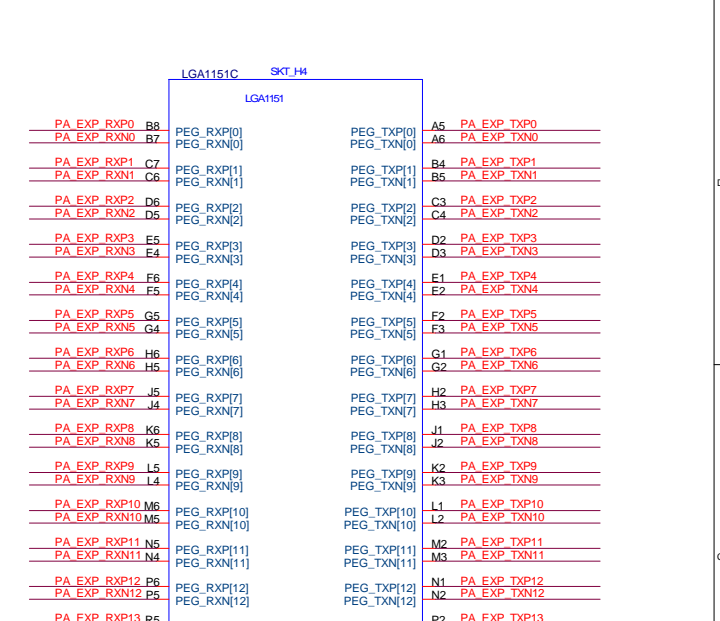
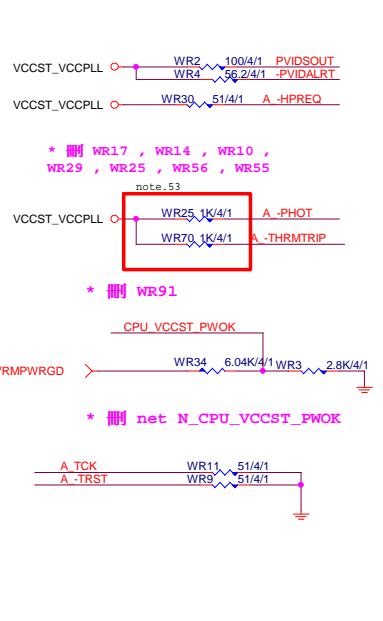
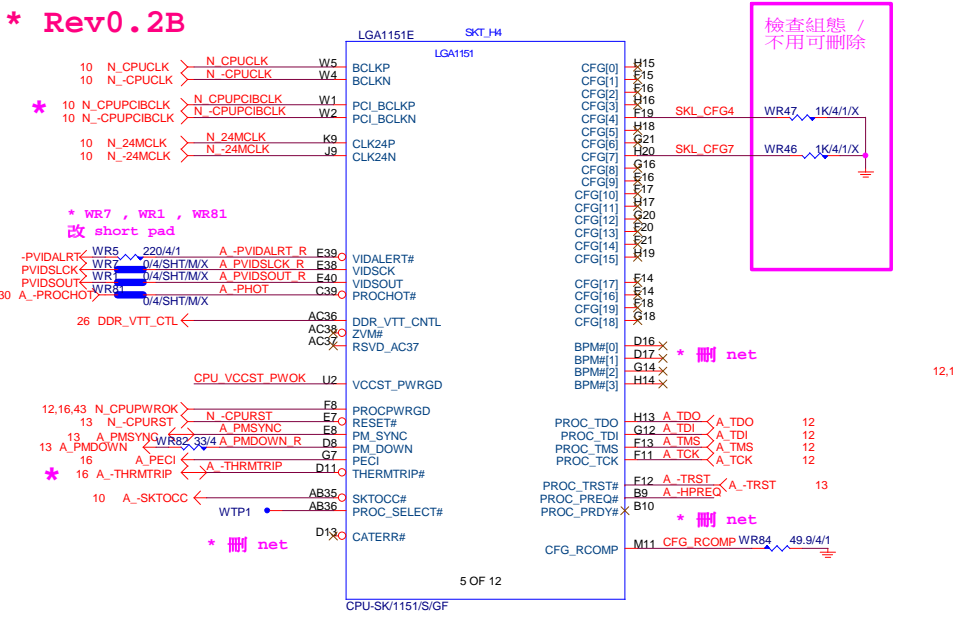
2015/09/04

[illegible][illegible]

BLOCK DIAGRAM



* Rev0.2B



G-15u : (CPU-SK/1151/S/15)
10SC1-F01151-11R / 10SC1-F01151-12R
G-FL : (CPU-SK/1151/S/GF)
10SC1-F01151-21R / 10SC1-F01151-22R

4 layer HDMI/DP/eDP/=====4/4/4//15
6 layer HDMI/DP/eDP/=====4/5.5/4//15

Impedance=85 +- 15%

enable:1:disable/0=enable
CFG[6:5]:PCI Express* Bifurcation; 1l= 1 x16 PCI Express;10=2x8 PCI Express
CFG[7]: PEG Training;1=(default) PEG Train immediately following RESET#;0=PEG Wait for BIOS

Bifurcation Config.	Signals	Lanes	
	CFG[6]	CFG[5]	CFG[2]
1x16	1	1	1
1x16 Reversed	1	1	0
2x8	1	0	1
2x8 Reversed	1	0	0
1x8+2x4	0	0	1
1x8+2x4 Reversed	0	0	0

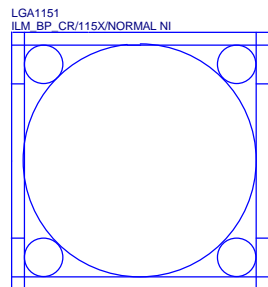
4 layer PEG/DMI=====4/4/4//15
6 layer PEG/DMI=====4/5.5/4//15

Impedance=85 +- 15%

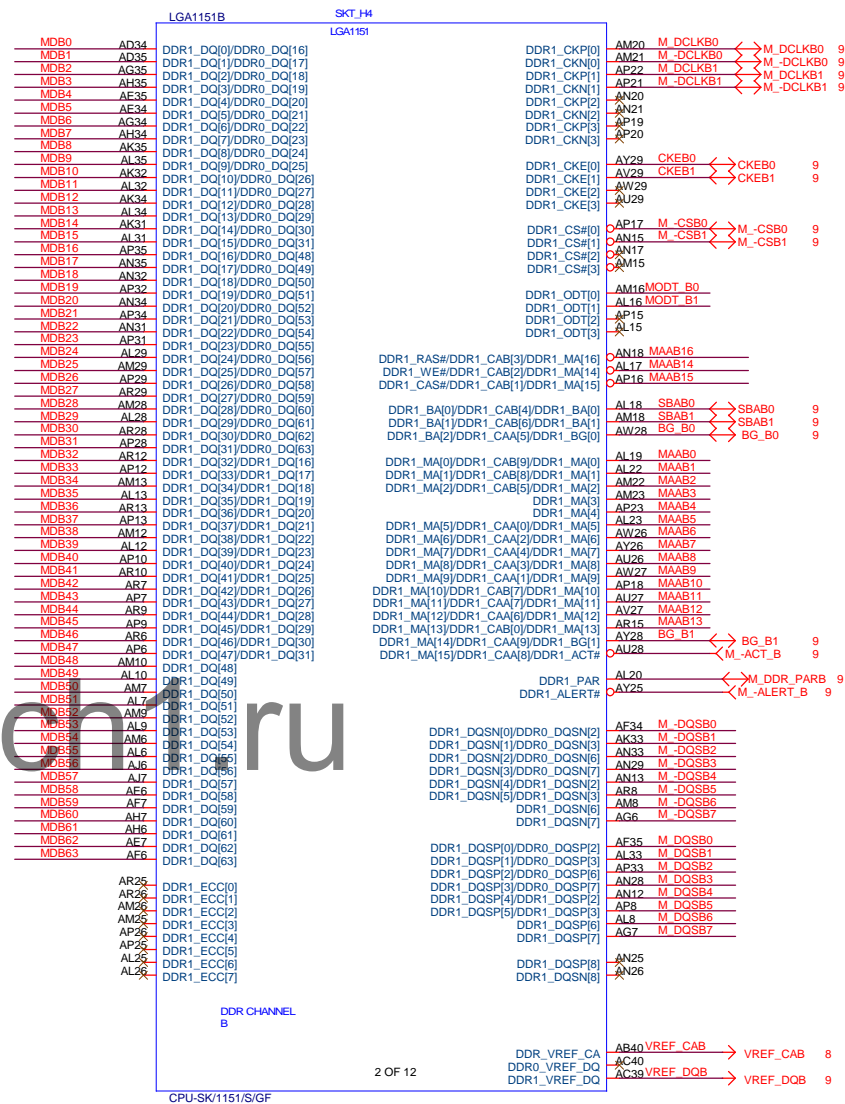
W=12 mil out of CPU
S=15 mil out of CPU

Gigabyte Technology		
CPU LGA1151-A		
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* 改DDR4 net



Need check the new CPU ME



8 MODT A[0..1] \longleftrightarrow MODT A[0..1]

9 MODT B[0..1] \longleftrightarrow MODT B[0..1]

8 MDA[0..63] ↔ MDA[0..63]

9 $\text{MDB}[0..63] \longleftrightarrow \text{MDB}[0..63]$

8 M_DQSA[0..7] \longleftrightarrow M_DQSA[0..7]

8 M_-DQSA[0..7] \longleftrightarrow M_-DQSA[0..7]

8 MAAA[0..16] \longleftrightarrow MAAA[0..16]

9 MAAB[0..16] \longleftrightarrow MAAB[0..16]

9 M_DQSB[0..7] \longleftrightarrow M_DQSB[0..7]

9 M_-DQSB[0..7] \longleftrightarrow M_-DQSB[0..7]

DDR CHANNEL
B

2 OF 12

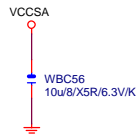
DDR_VREF_CA	AB40	VREF_CAB	→	VREF_CAB	8
DDR0_VREF_DQ	AC40				
DDR1_VREF_DQ	AC39	VREF_DQB	→	VREF_DQB	9

Gigabyte Technology

CPU LGA1151-B

Size Custom	Document Number	GA-H110M-DS2	Rev 1.0
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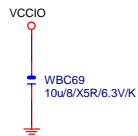
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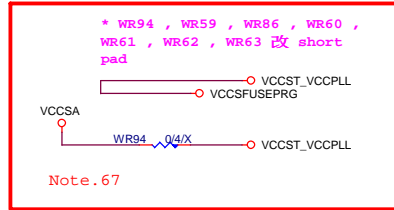
* 刪 WBC50 電容

* WBC51 , WBC52
VDDQ 改 VCCSA

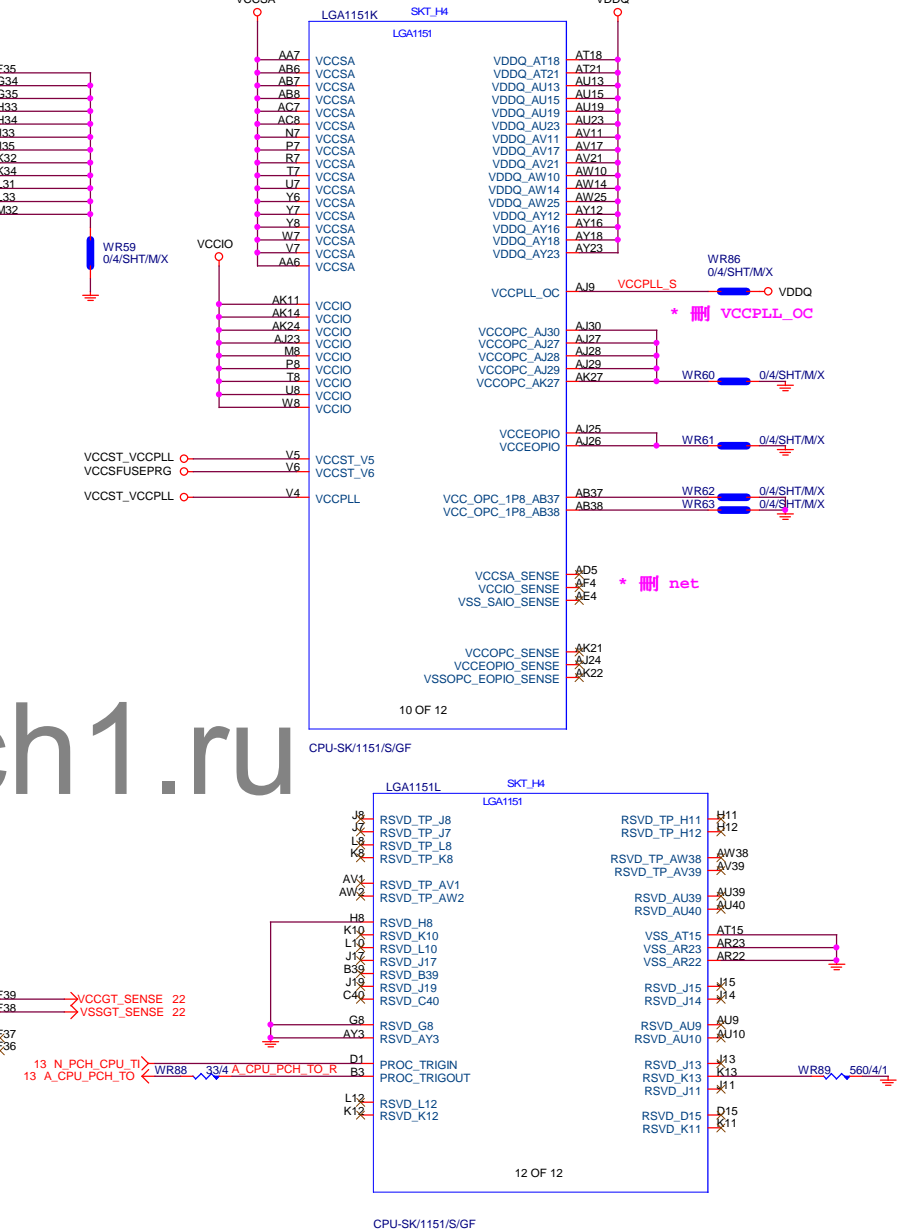
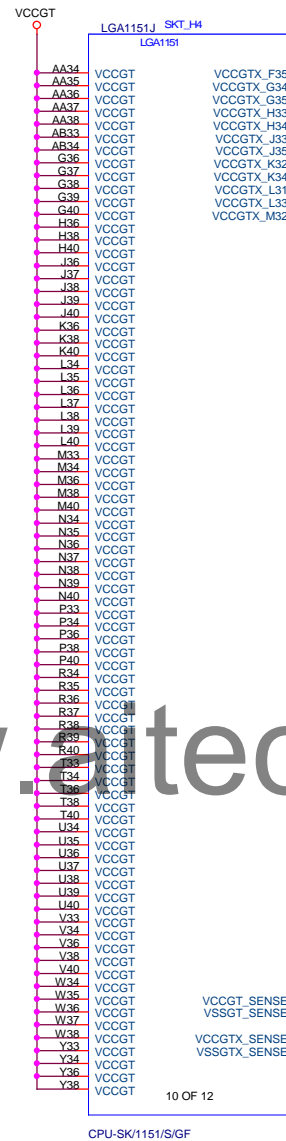
* 刪 WBC124 , WBC125 , WBC126 , WBC127 電容

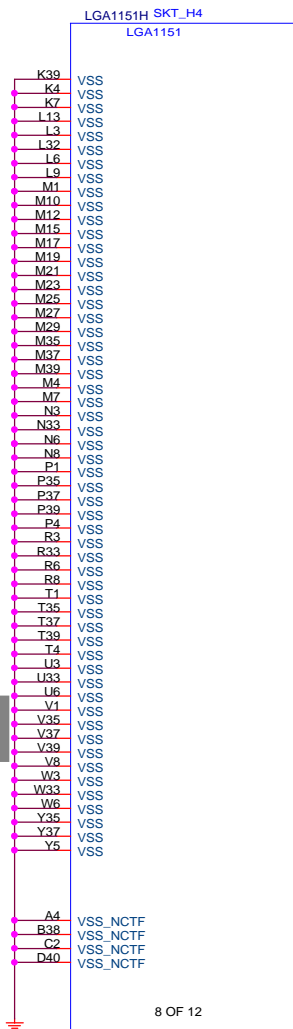
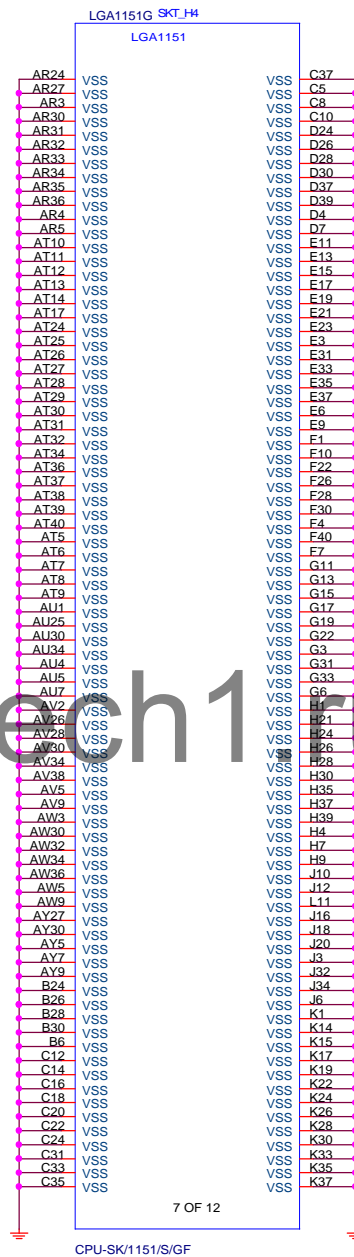
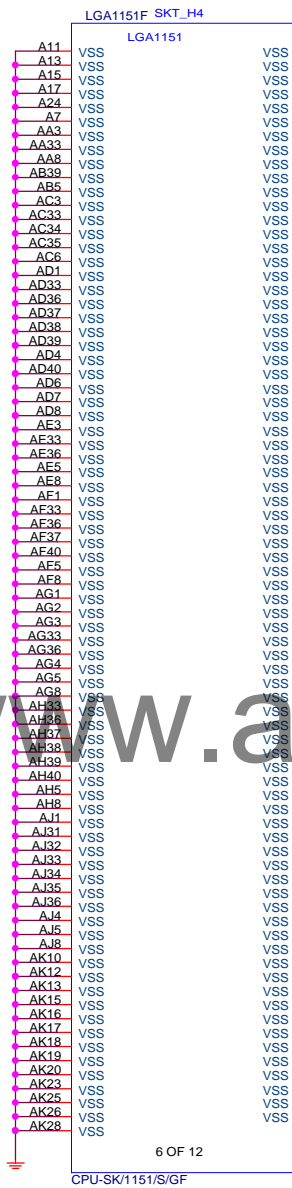
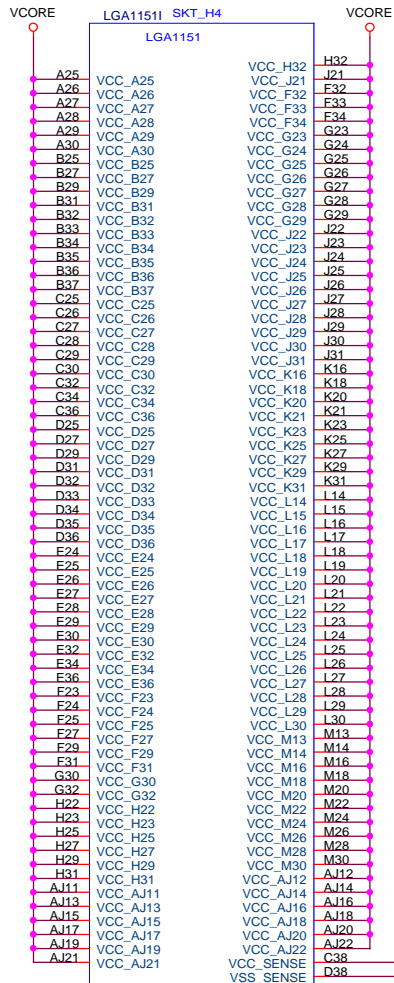


* 刪 VCCGT 電容

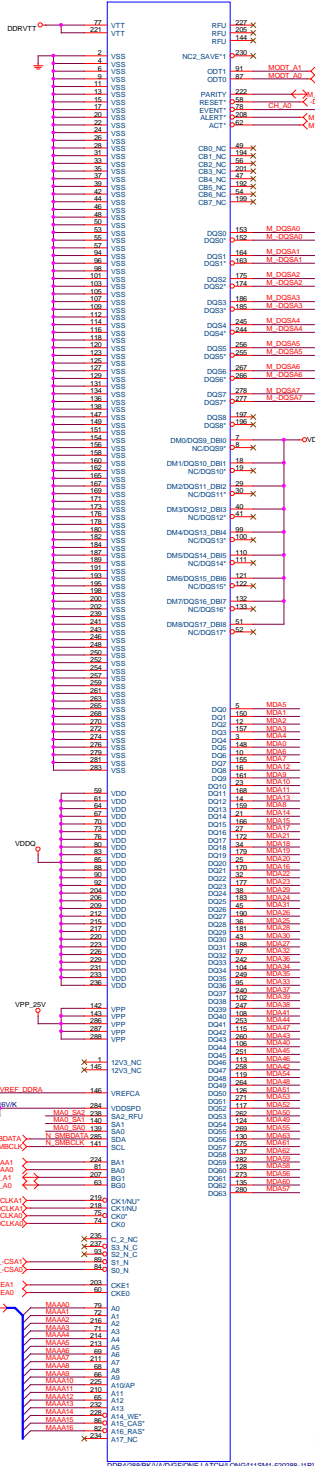


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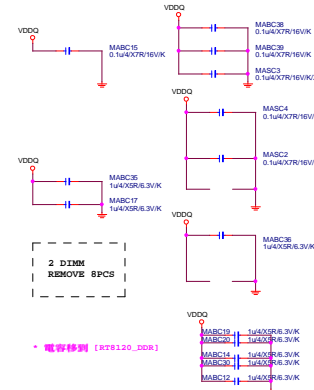
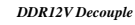
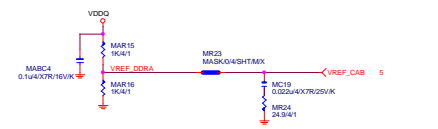




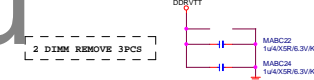
* 刪 Vcore 電容



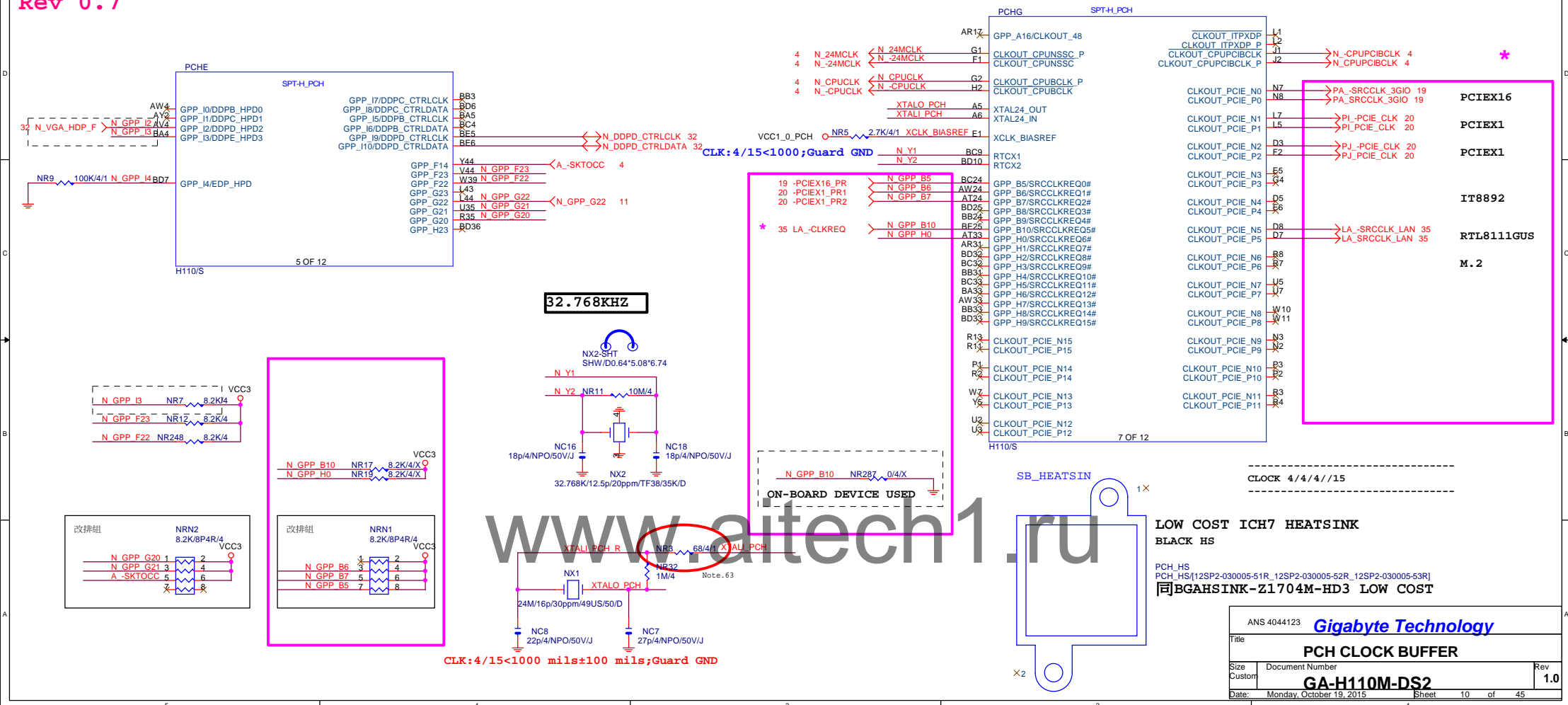
CHANNEL A0
SA2:0=000

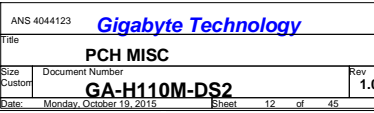


DDRVTT Decouple



- 副電容

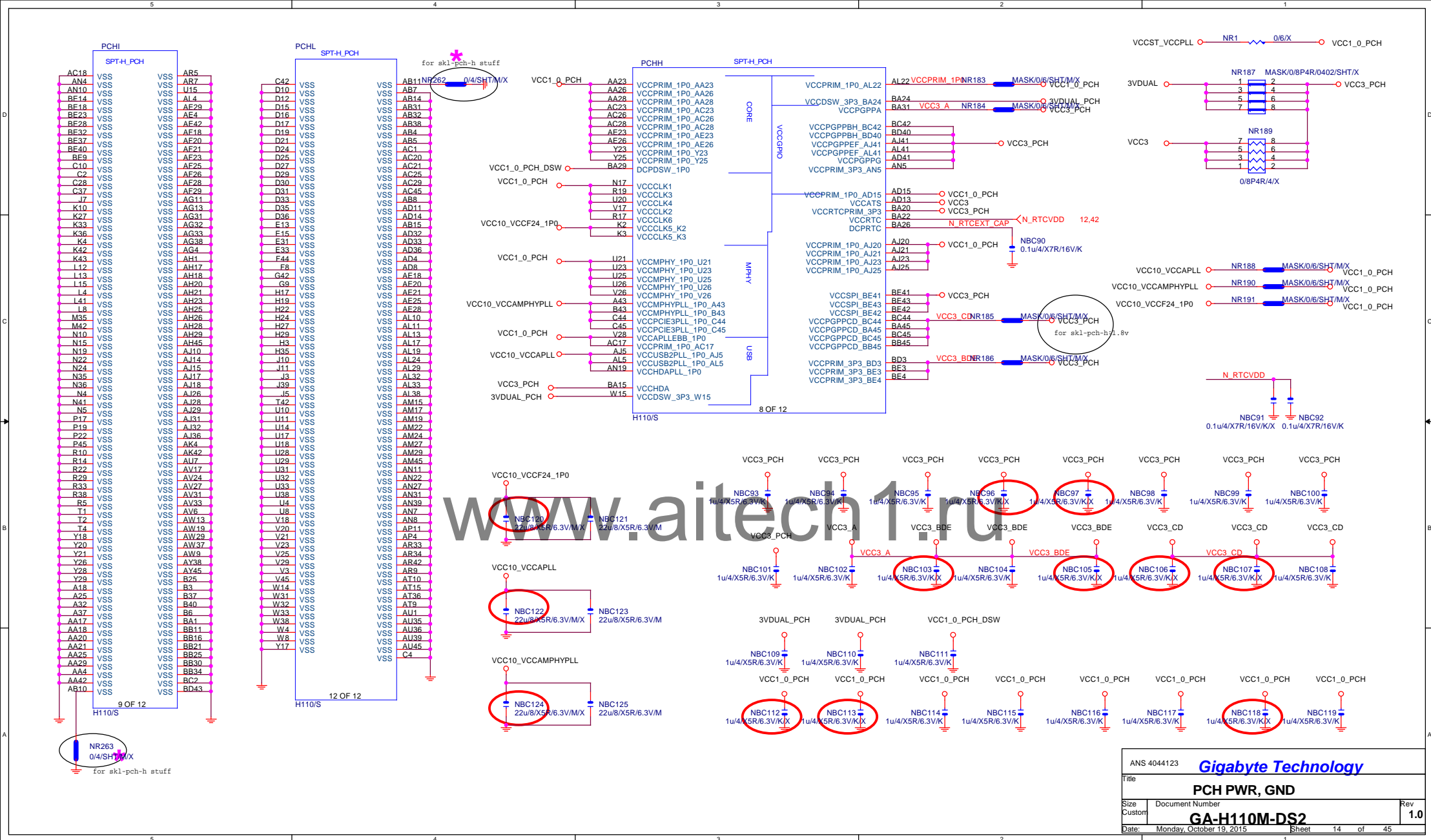


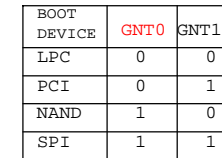




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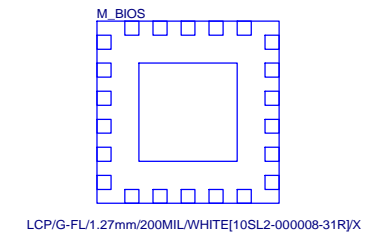
ANS 4044123		Gigabyte Technology	
Title		PCH SATA,PCIE,SATA_EXPRESS	
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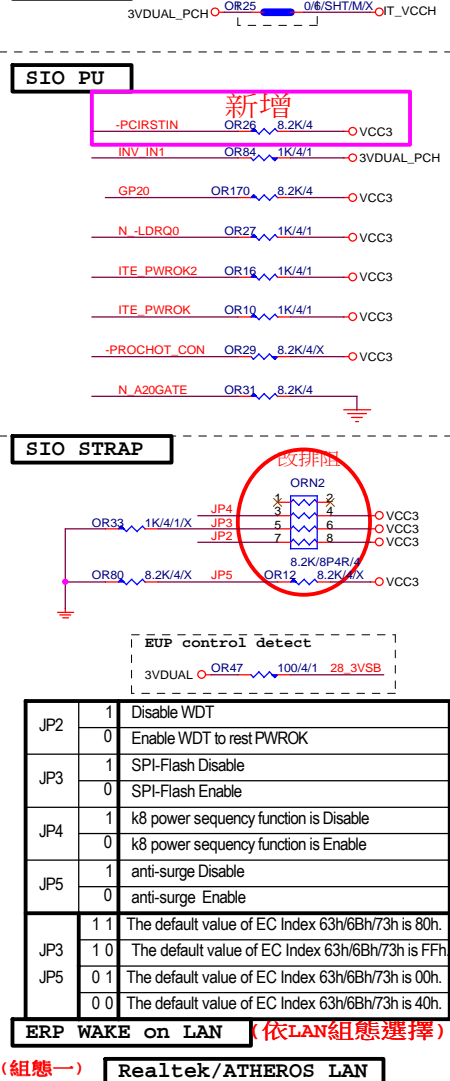
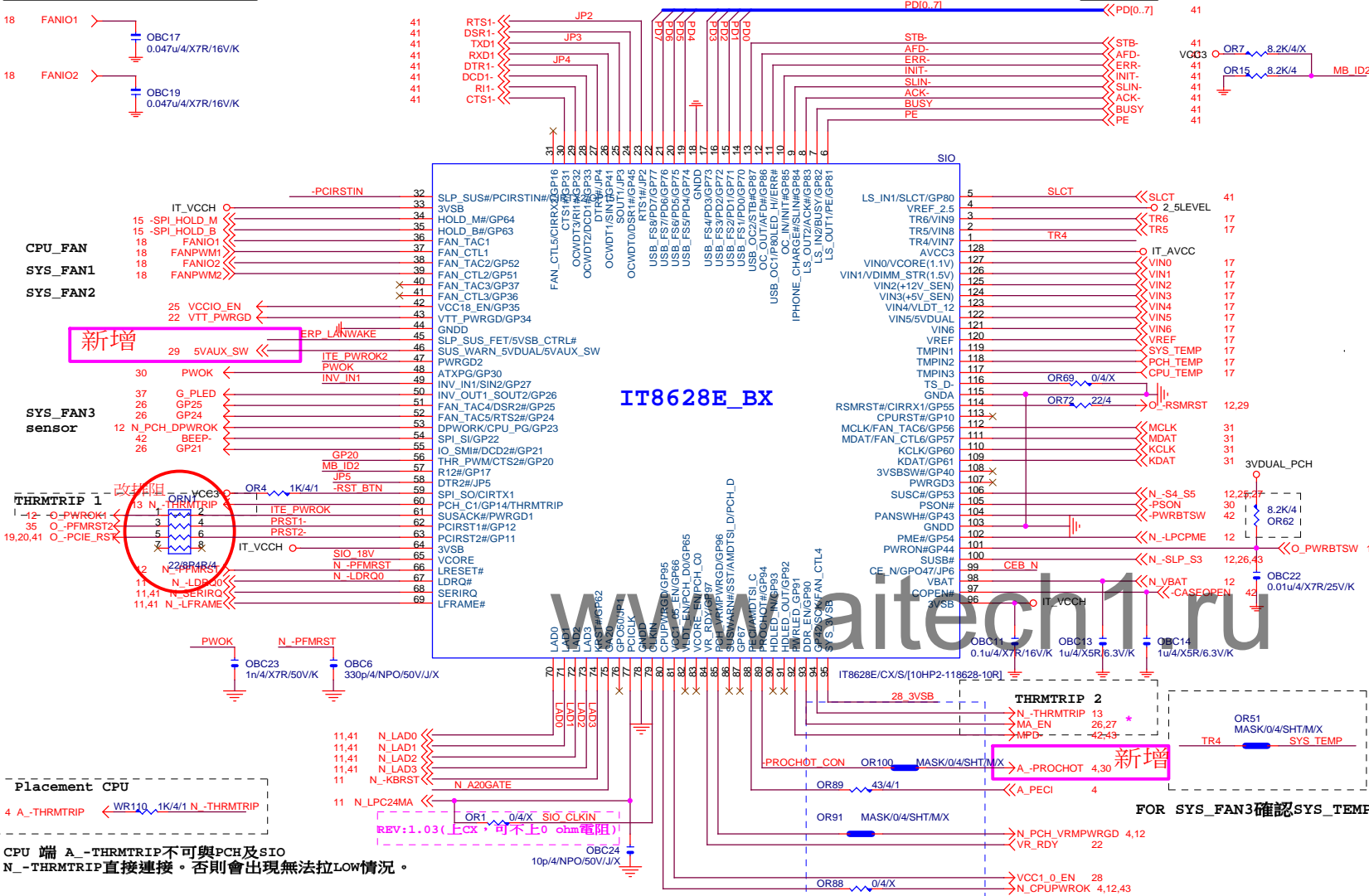
1 means floating
0 means PD 1K

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* 試產先上，PVT 移除

BIOS_PH



JP2	1	Disable WDT
JP2	0	Enable WDT to rest PWROK
JP3	0	SPI-Flash Disable
JP3	1	SPI-Flash Enable
JP4	1	k8 power sequency function is Disable
JP4	0	k8 power sequency function is Enable
JP5	1	anti-surge Disable
JP5	0	anti-surge Enable
JP3	1 1	The default value of EC Index 63h/6Bh/73h is 80h.
JP3	1 0	The default value of EC Index 63h/6Bh/73h is FFh
JP5	0 1	The default value of EC Index 63h/6Bh/73h is 00h.
JP5	0 0	The default value of EC Index 63h/6Bh/73h is 40h.

ERP WAKE on LAN (依LAN組態選擇)
(組態一)

FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL5 FAN_TAC5
OPT_FAN or SYS_FAN4	N/A
THRMTRIP1	YES PIN60
THRMTRIP2	YES PIN94

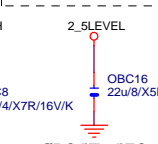
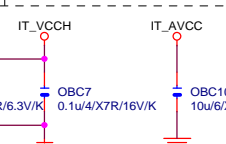
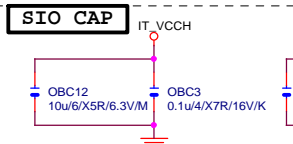
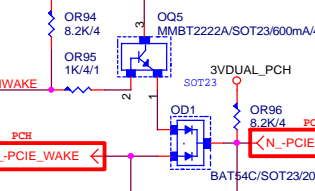
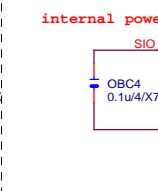
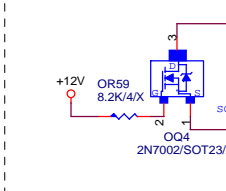
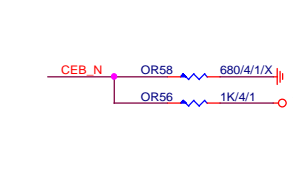
IT8620E GPIO問題匯整	
PIN 50	GP26-第一次接上POWER時 會拉 Lo
PIN 90/91	DEFAULT為HDLed FUNCTION, GP93 BYPASS TO GP92 高溫時 GP92 會被拉Lo(ITE BUG)
PIN 108	GP40--- POWER ON 時會拉 Lo
PIN 111/112	MOUSE 跟FAN6 FUNCTION 擇一使用,不然會互相干擾
PIN 22	PIN22, 需高於3V, 若低於 該部分COM PORT及LET裝置 蜂鳴器會異常動作。

DUAL BIOS OPT STRAP

Power leakage

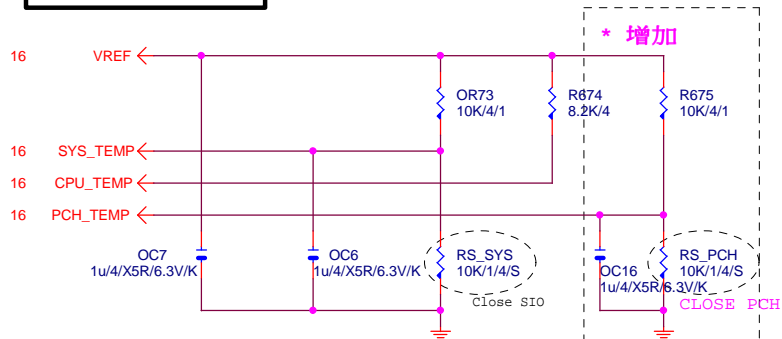
SIO_18V

Realtek/ATHEROS LAN

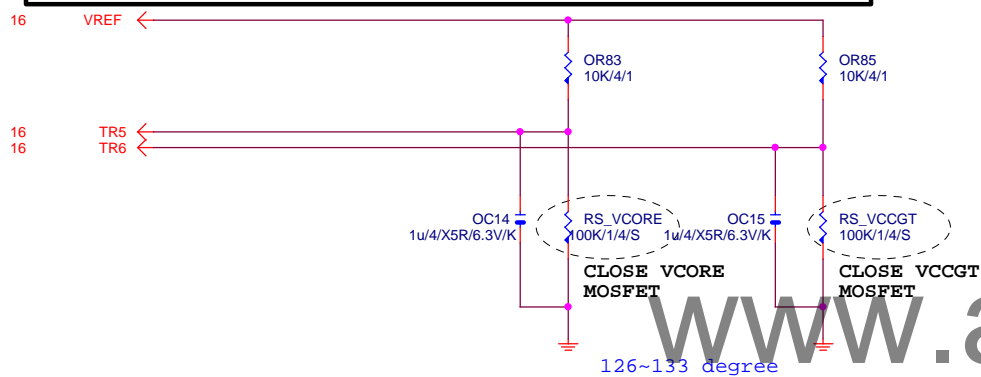


TEMP H/W MONITOR

REV 1.04



RS_VCORE ~ RS_VCCGT CLOSE CPU_VCORE & VCCGT MOSFET

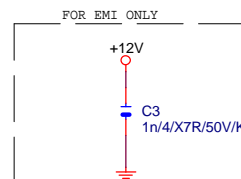
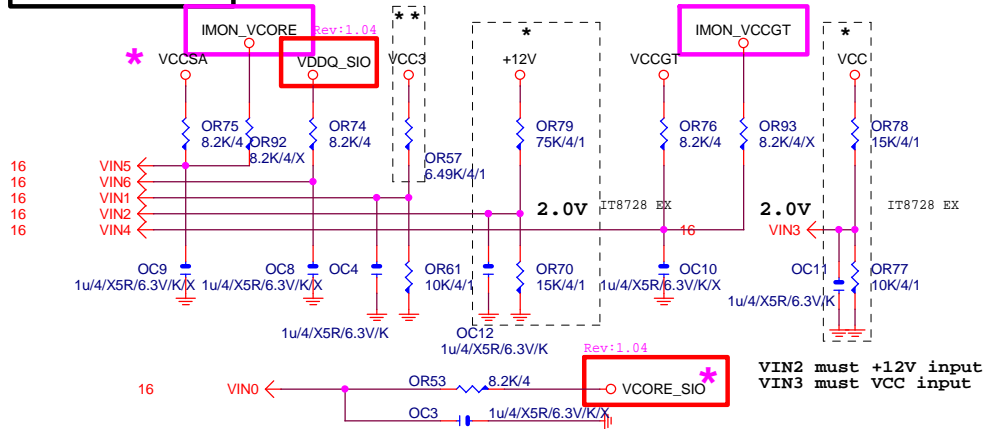


VOLTAGE-- H/W MONITOR

Connect to PWM

* IT8728 BX
** IT8728 CX

Connect to PWM

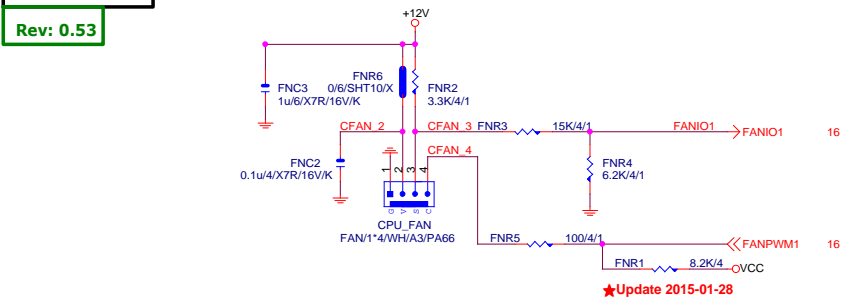


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Title			HWM,KB/MS, FAN CTRL		
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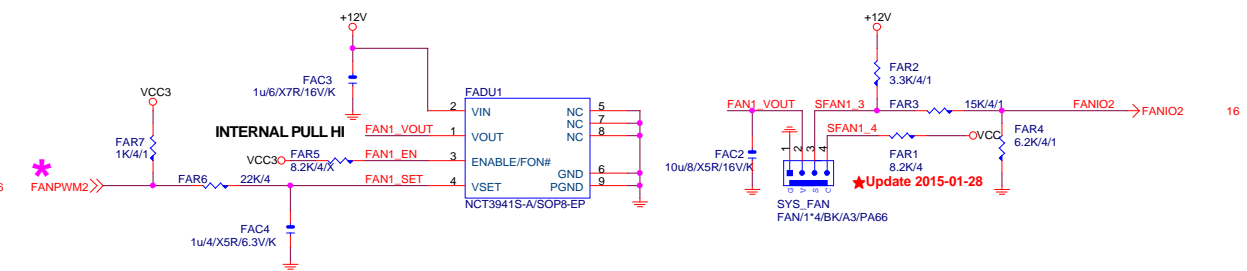
CPU SMART FAN

Rev: 0.53



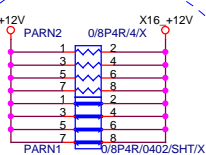
SYSTEM FAN1

A.
Linear SYS_FAN
Enable Function (NCT3941S)
Full Turn On Function (NCT3941S-A)



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Rev 0.2

+12V_protect
short-wire test

PA_EXP_RXP0_15] >> PA_EXP_RXP0_15] 4
 PA_EXP_RXN0_15] >> PA_EXP_RXN0_15] 4
 PA_EXP_TXP0_15] >> PA_EXP_TXP0_15] 4
 PA_EXP_TXN0_15] >> PA_EXP_TXN0_15] 4

PA_EXP_TXP0	PAC5	0.22u4/X5R/6.3V/K	PA_EXP_TXP0 C
PA_EXP_TXN0	PAC4	0.22u4/X5R/6.3V/K	PA_EXP_TXN0 C
PA_EXP_TXP1	PAC6	0.22u4/X5R/6.3V/K	PA_EXP_TXP1 C
PA_EXP_TXN1	PAC7	0.22u4/X5R/6.3V/K	PA_EXP_TXN1 C
PA_EXP_TXP2	PAC8	0.22u4/X5R/6.3V/K	PA_EXP_TXP2 C
PA_EXP_TXN2	PAC9	0.22u4/X5R/6.3V/K	PA_EXP_TXN2 C
PA_EXP_TXP3	PAC10	0.22u4/X5R/6.3V/K	PA_EXP_TXP3 C
PA_EXP_TXN3	PAC11	0.22u4/X5R/6.3V/K	PA_EXP_TXN3 C
PA_EXP_TXP4	PAC12	0.22u4/X5R/6.3V/K	PA_EXP_TXP4 C
PA_EXP_TXN4	PAC13	0.22u4/X5R/6.3V/K	PA_EXP_TXN4 C
PA_EXP_TXP5	PAC14	0.22u4/X5R/6.3V/K	PA_EXP_TXP5 C
PA_EXP_TXN5	PAC15	0.22u4/X5R/6.3V/K	PA_EXP_TXN5 C
PA_EXP_TXP6	PAC16	0.22u4/X5R/6.3V/K	PA_EXP_TXP6 C
PA_EXP_TXN6	PAC17	0.22u4/X5R/6.3V/K	PA_EXP_TXN6 C
PA_EXP_TXP7	PAC18	0.22u4/X5R/6.3V/K	PA_EXP_TXP7 C
PA_EXP_TXN7	PAC19	0.22u4/X5R/6.3V/K	PA_EXP_TXN7 C
PA_EXP_TXP8	PAC20	0.22u4/X5R/6.3V/K	PA_EXP_TXP8 C
PA_EXP_TXN8	PAC21	0.22u4/X5R/6.3V/K	PA_EXP_TXN8 C
PA_EXP_TXP9	PAC22	0.22u4/X5R/6.3V/K	PA_EXP_TXP9 C
PA_EXP_TXN9	PAC23	0.22u4/X5R/6.3V/K	PA_EXP_TXN9 C
PA_EXP_TXP10	PAC24	0.22u4/X5R/6.3V/K	PA_EXP_TXP10 C
PA_EXP_TXN10	PAC25	0.22u4/X5R/6.3V/K	PA_EXP_TXN10 C
PA_EXP_TXP11	PAC26	0.22u4/X5R/6.3V/K	PA_EXP_TXP11 C
PA_EXP_TXN11	PAC27	0.22u4/X5R/6.3V/K	PA_EXP_TXN11 C
PA_EXP_TXP12	PAC28	0.22u4/X5R/6.3V/K	PA_EXP_TXP12 C
PA_EXP_TXN12	PAC29	0.22u4/X5R/6.3V/K	PA_EXP_TXN12 C
PA_EXP_TXP13	PAC30	0.22u4/X5R/6.3V/K	PA_EXP_TXP13 C
PA_EXP_TXN13	PAC31	0.22u4/X5R/6.3V/K	PA_EXP_TXN13 C
PA_EXP_TXP14	PAC32	0.22u4/X5R/6.3V/K	PA_EXP_TXP14 C
PA_EXP_TXN14	PAC33	0.22u4/X5R/6.3V/K	PA_EXP_TXN14 C
PA_EXP_TXP15	PAC34	0.22u4/X5R/6.3V/K	PA_EXP_TXP15 C
PA_EXP_TXN15	PAC35	0.22u4/X5R/6.3V/K	PA_EXP_TXN15 C

PCIE16:16/5/5/5/16

PCI-E REV:1.1--> 2.5GHZ

PCE-E X1(單向) BANDWIDTH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

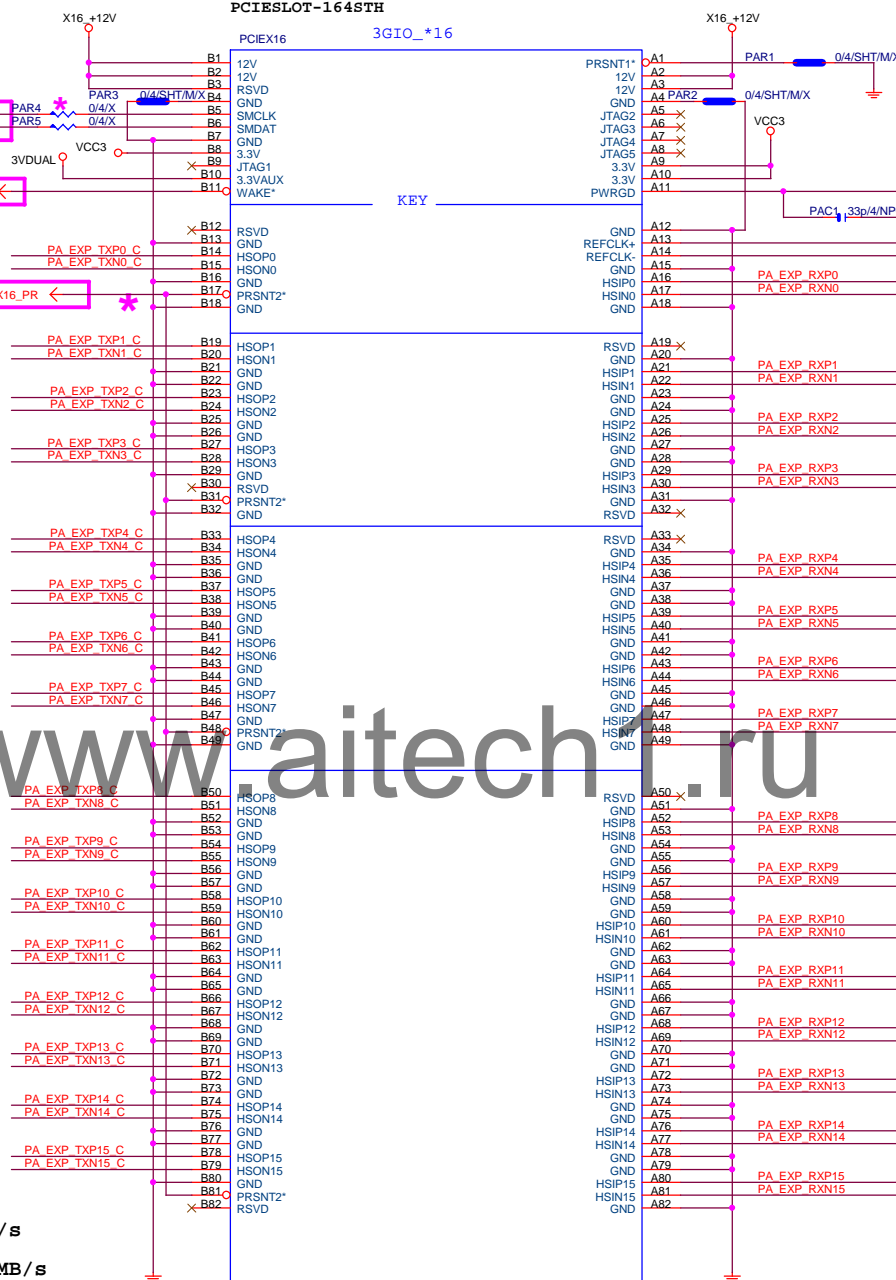
PCE-E X1(雙向) BANDWIDTH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

PCE-E X16(單向) BANDWIDTH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

PCE-E X16(雙向) BANDWIDTH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ

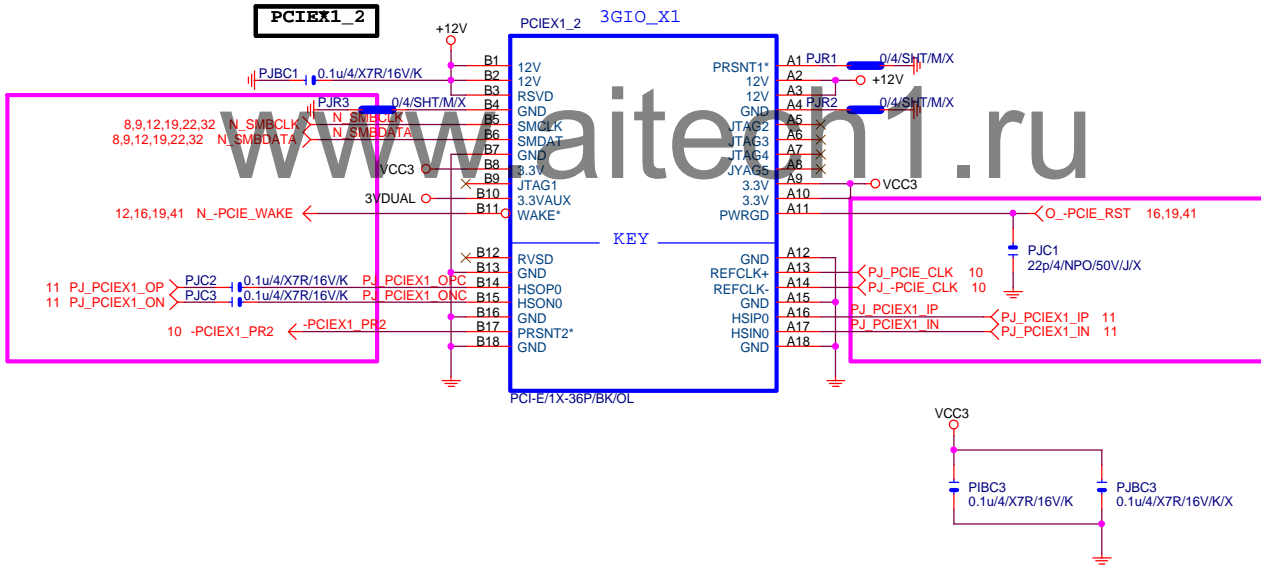
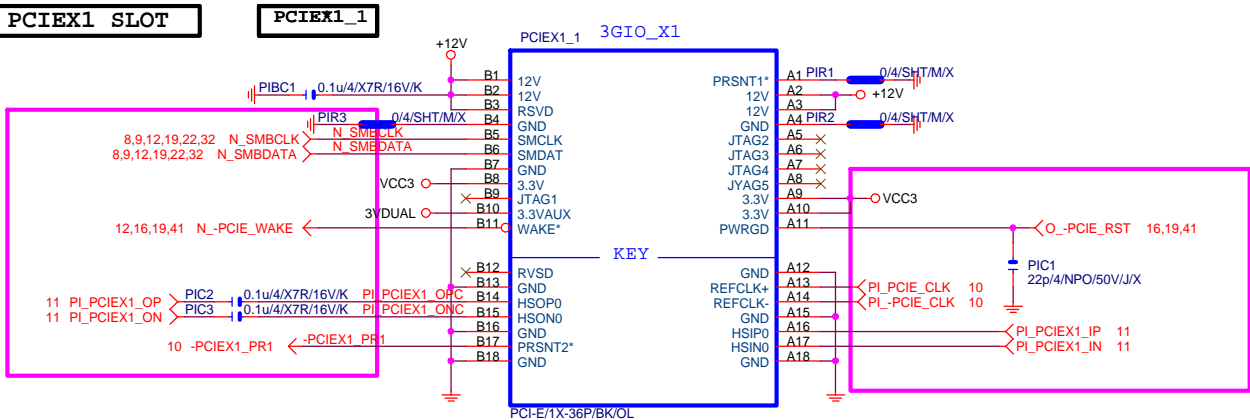
PCIESLOT-1645TH



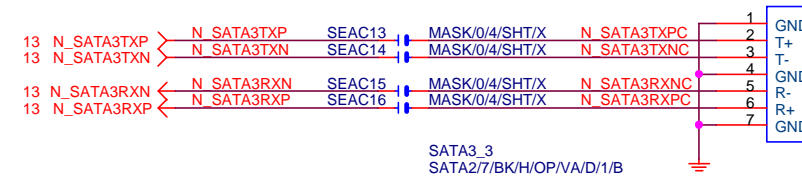
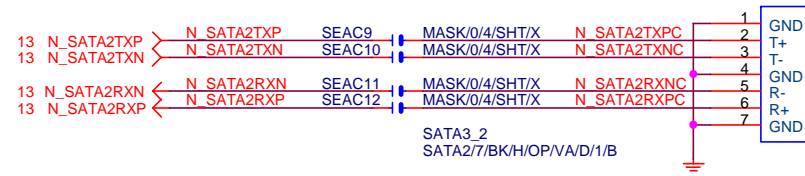
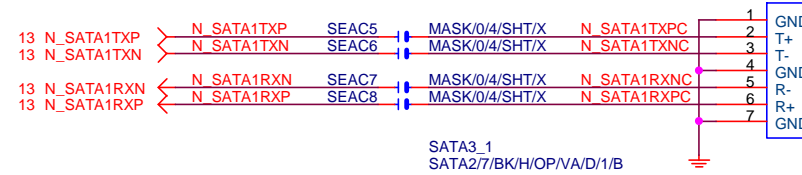
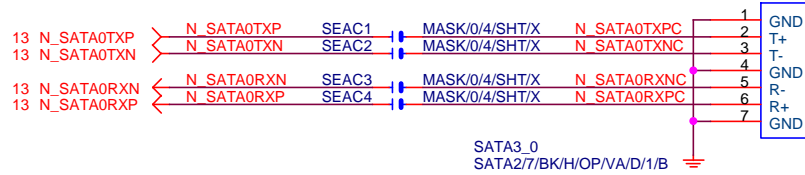
PCI-E/16X-164P/GY/LONG DOUBLE/HK*2

Gigabyte Technology

Title			PCI EXPRESS * 16	
Size			Document Number	
Custom			GA-H110M-DS2	
Date:			Monday, October 19, 2015	
			Sheet 19 of 46	
			Rev 1.0	

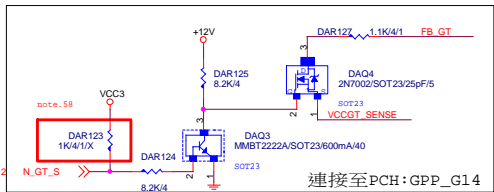
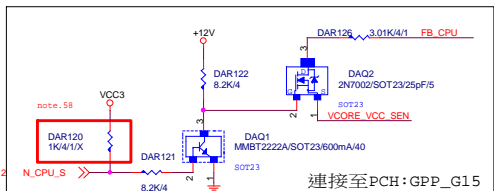
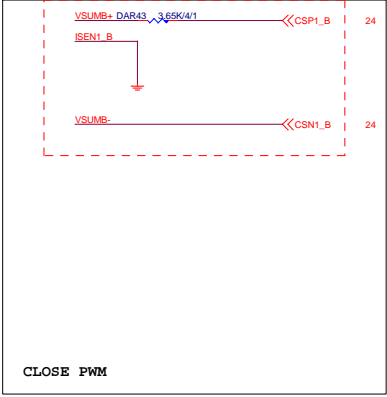
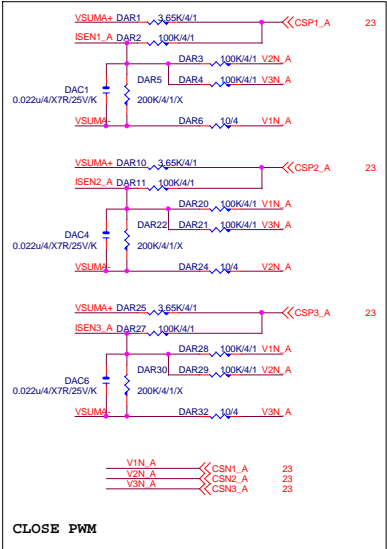
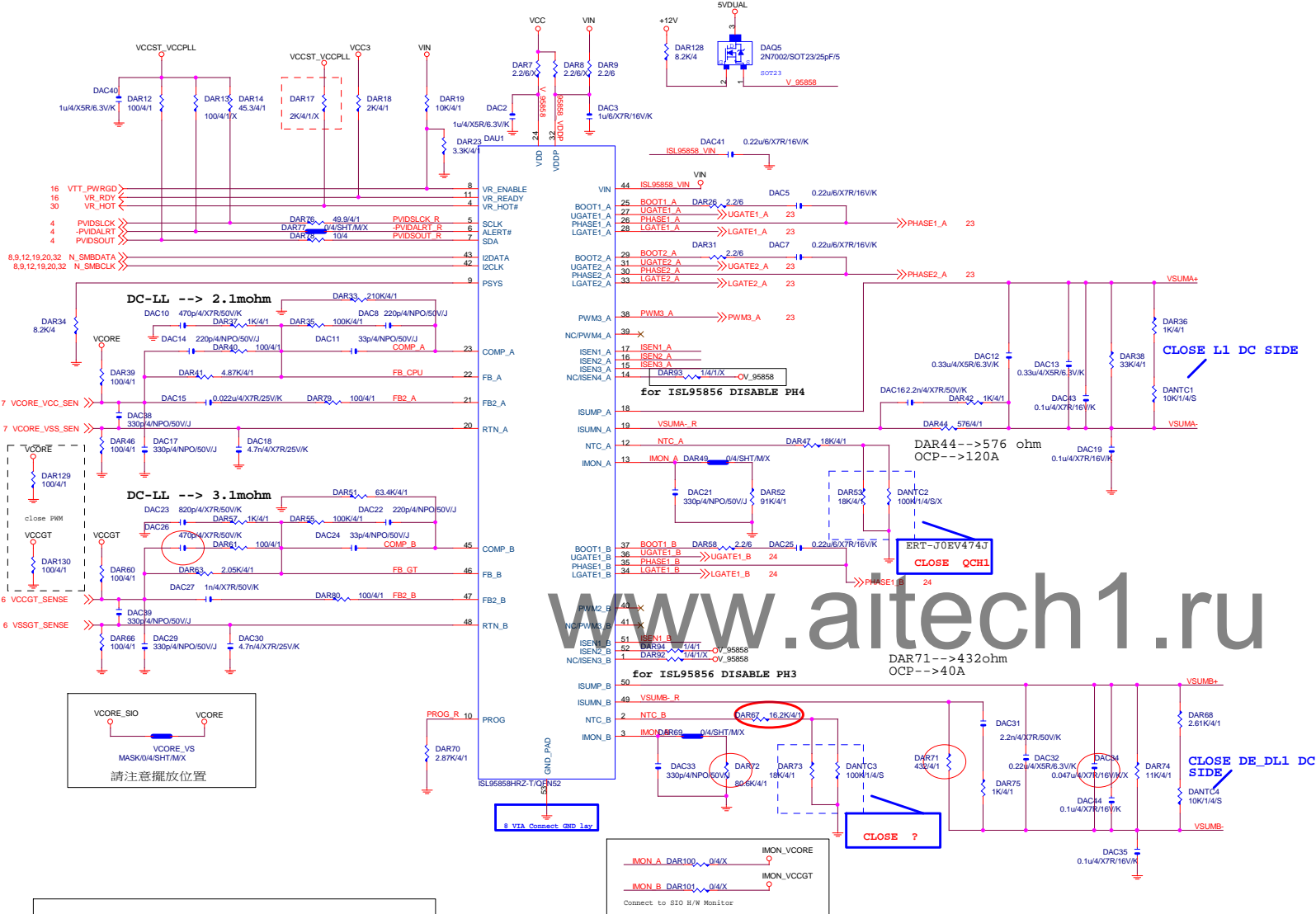


Rev 0.6



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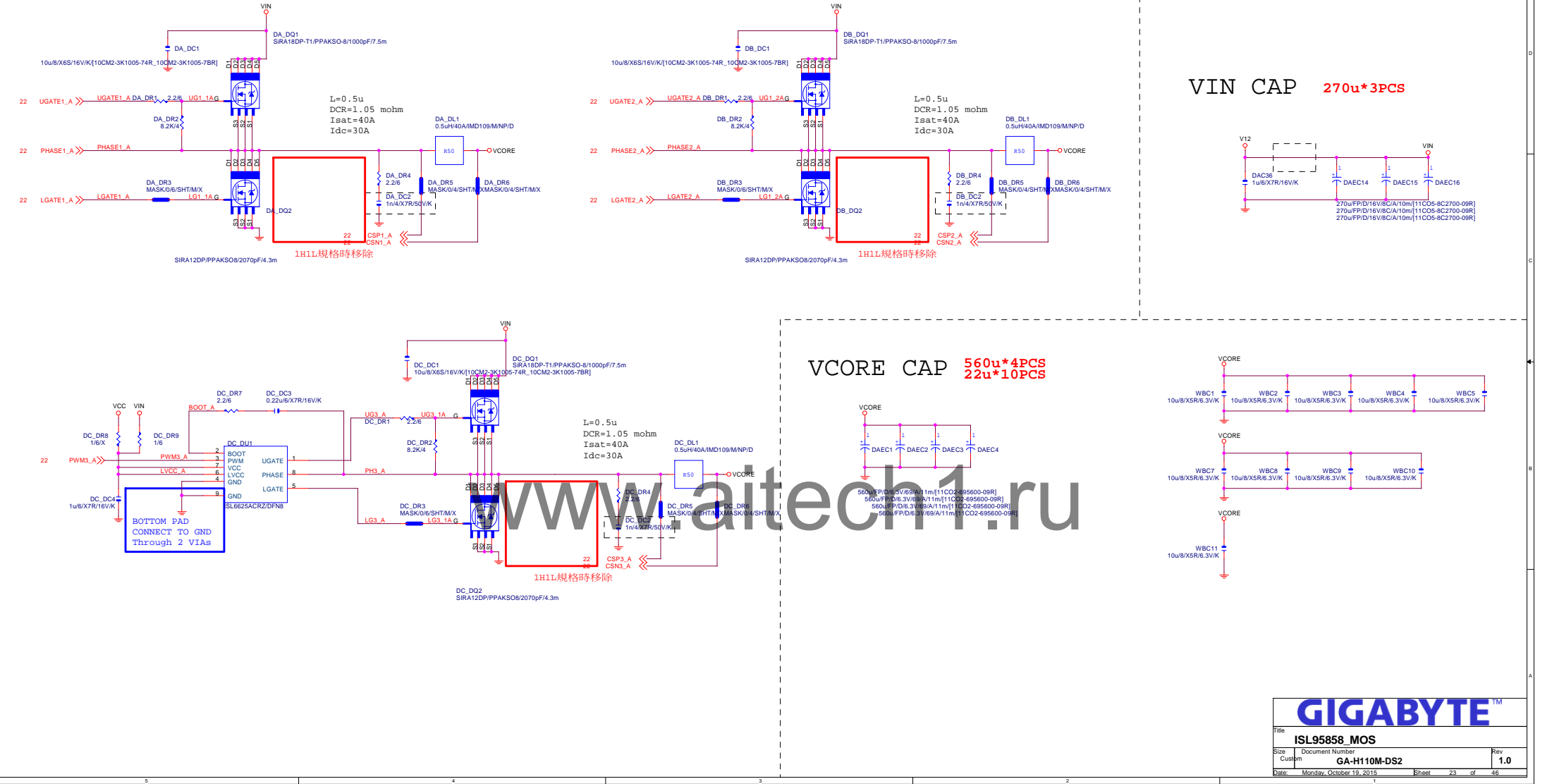
Gigabyte Technology			
Title			
SATA EXPRESS			
Size	Document Number		Rev
Custom	GA-H110M-DS2		1.0
Date:	Monday, October 19, 2015	Sheet	21 of 46



REV:0.91

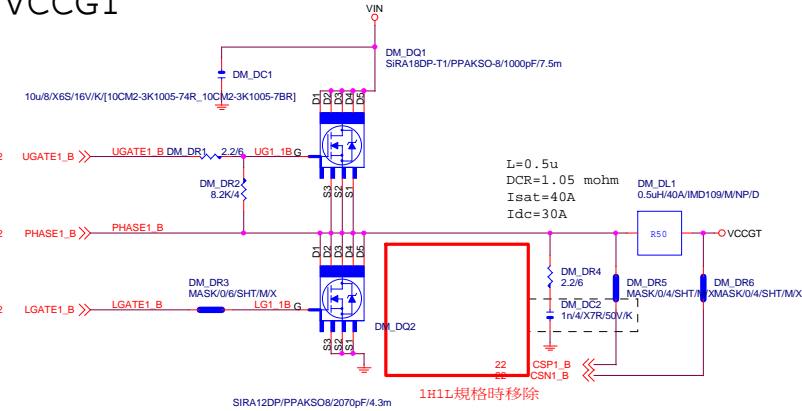
REV:0.15

VCORE

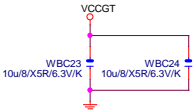
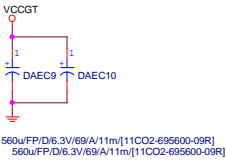


GIGABYTE™			
Title ISL95858_MOS			
Size	Document Number	Rev	
Custm	GA-H110M-DS2	1.0	
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VCCGT



VCCGT CAP 560u*2PCS
22u*2PCS



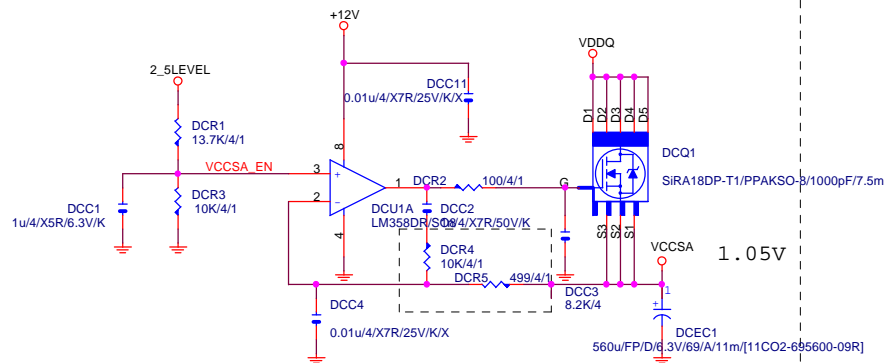
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GIGABYTE™

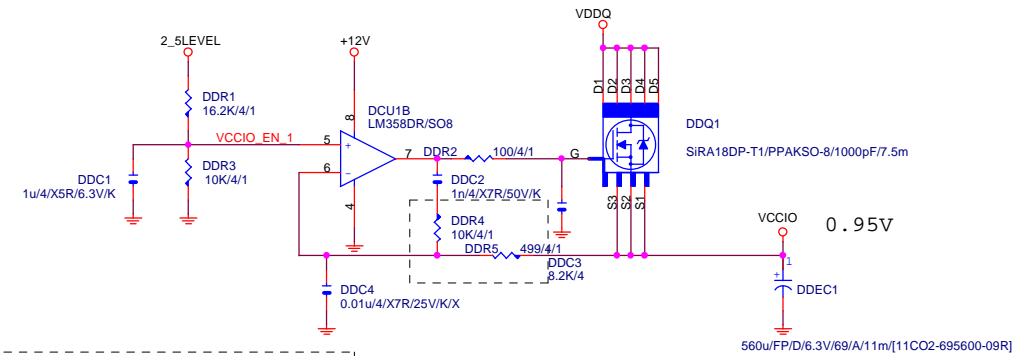
Title			ISL95858_MOS	
Size			Document Number	Rev
Custom			GA-H110M-DS2	1.0
Date:			Monday, October 19, 2015	Sheet 24 of 46

VCCSA

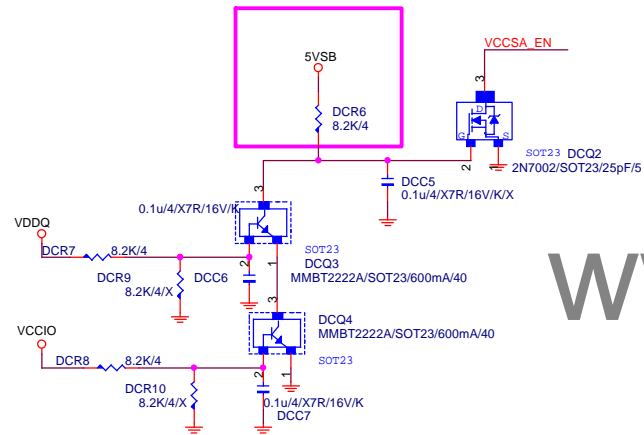
REV:0.4



VCCIO

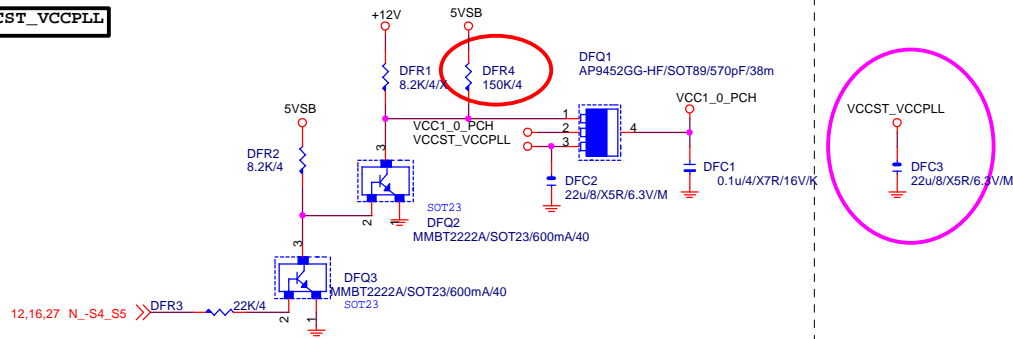


VCCIO_EN_1 DDR10 0/4/SHT/M/X VCCIO_EN 16
Connect to IT8620



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VCCST_VCCPLL



GIGABYTE™			
Title VCCSA_VCCIO			
Size Custom	Document Number GA-H110M-DS2	Rev 1.0	
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REV:0.39

DDR4

DDR VIN CAP
560u*1PCS

CHOKE與CAP料號可變

上件

SUPPORT DDR4 1.2V

25A MAX

L=1u
DCR=2.5 mohm
Isat=35A
Idc=28A

Remote sense請從最重的負載端點拉回

MA_DR38.MA_DC15

VPP_25V使用8120.8068A.RT8237時上件

PWR SEQ

CLOSE TO DDR POWER PLANE

For power sequence require

VPP_25V使用8120時上件

DDR CAP 560u*4PCS 22u*2PCS

* 大電容 *4

DDRVTTCAP

* 大電容 *0

DDRVTTCAP

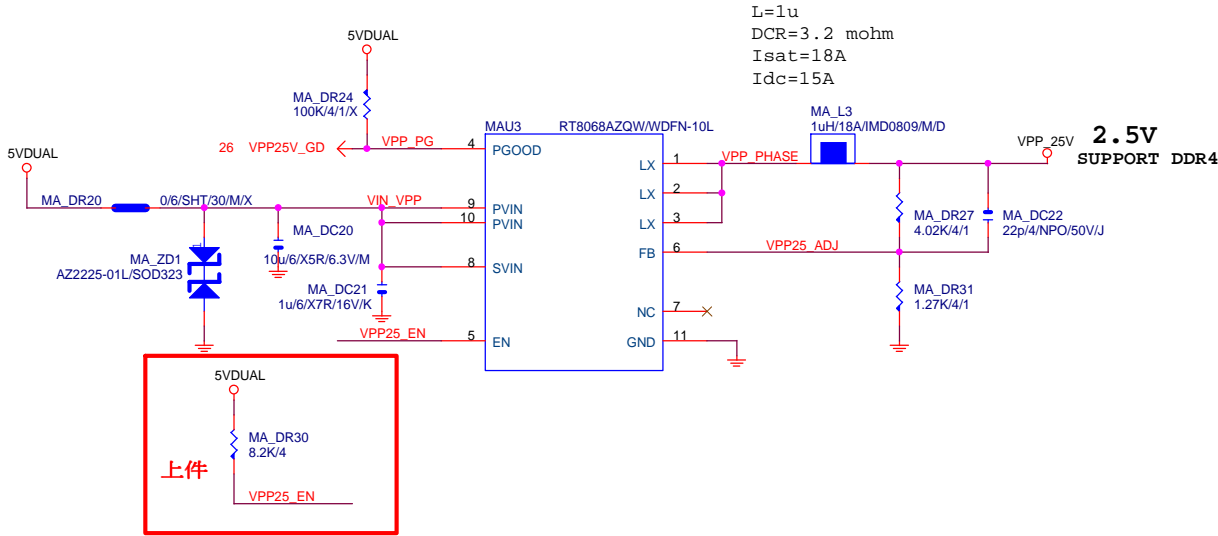
GIGABYTE™

Title		
RT8237_DDR4 POWER		
Size	Document Number	Rev
Custom	GA-H110M-DS2	1.0
Date:	Monday, October 19, 2015	Sheet 26 of 46

REV:0.4

VPP_25V

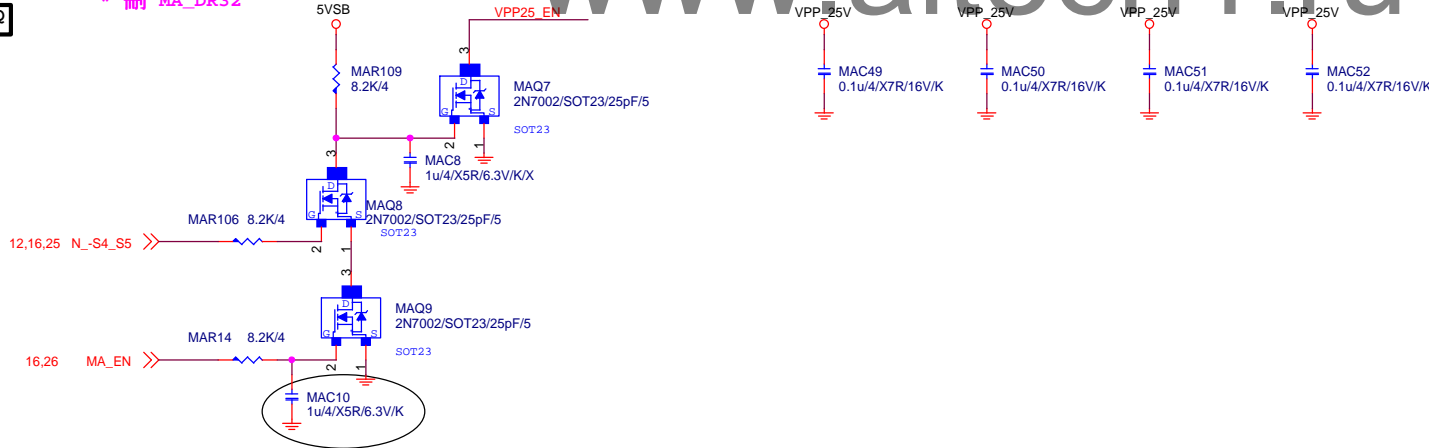
CHOKE與CAP料號可變



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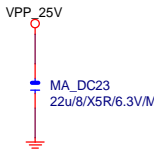
PWR_SEQ

* 刪 MA_DR32



VPP CAP 22u*1PCS

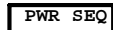
* 大電容 x0



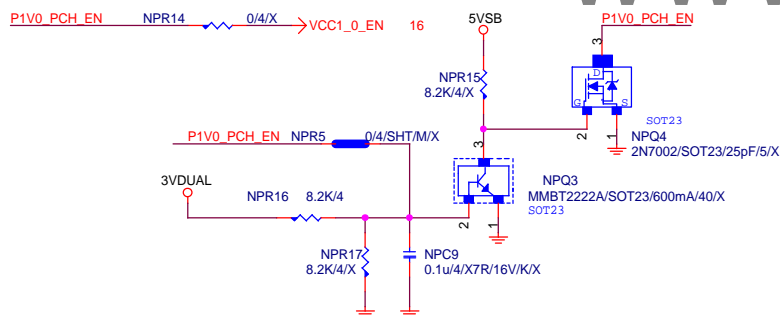
GIGABYTE™

Title		
RT9018_VPP25 POWER		
Size	Document Number	Rev
Custom	GA-H110M-DS2	1.0
Date:	Monday, October 19, 2015	Sheet 27 of 46

1
+
NPEC1
100u/OS/D/16V/69/A/35m/[110



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請放置CHOKE一出來的地方

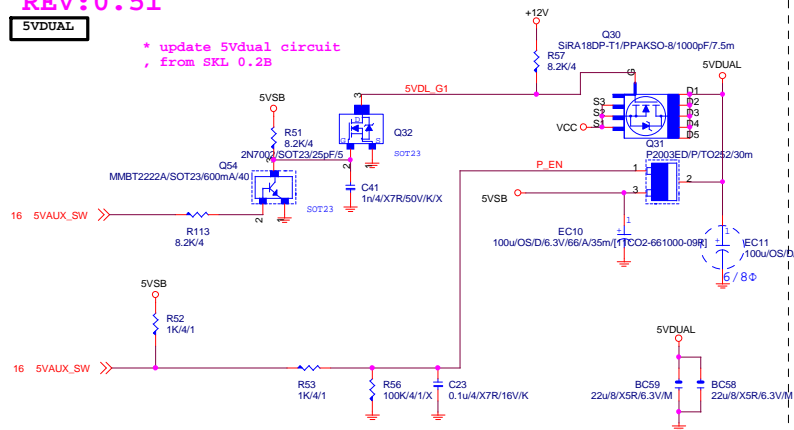
GIGABYTE™

Title			
RT8237_PCH POWER			
Size	Document Number	Rev	
Custom	GA-H110M-DS2	1.0	
Date:	Monday, October 19, 2015	Sheet	28 of 46

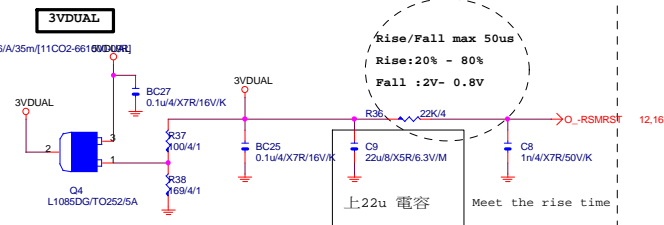
REV:0.51

5VDUAL

* update 5Vdual circuit
from SKL 0.2B



3VDUAL

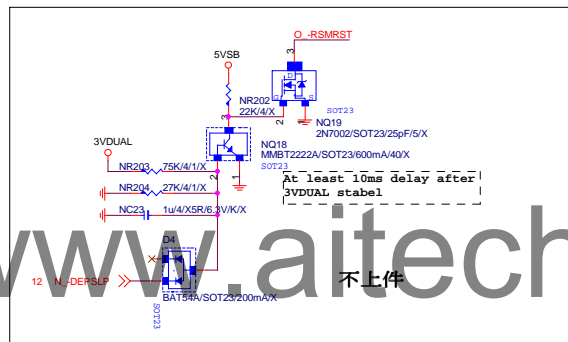
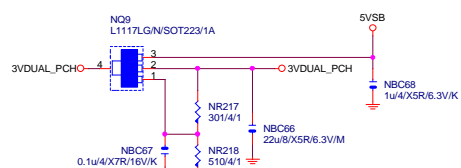


Rise/Fall max 50us
Rise:20% - 80%
Fall :2V- 0.8V

上22u 电容

Meet the rise time

3VDUAL_PCH



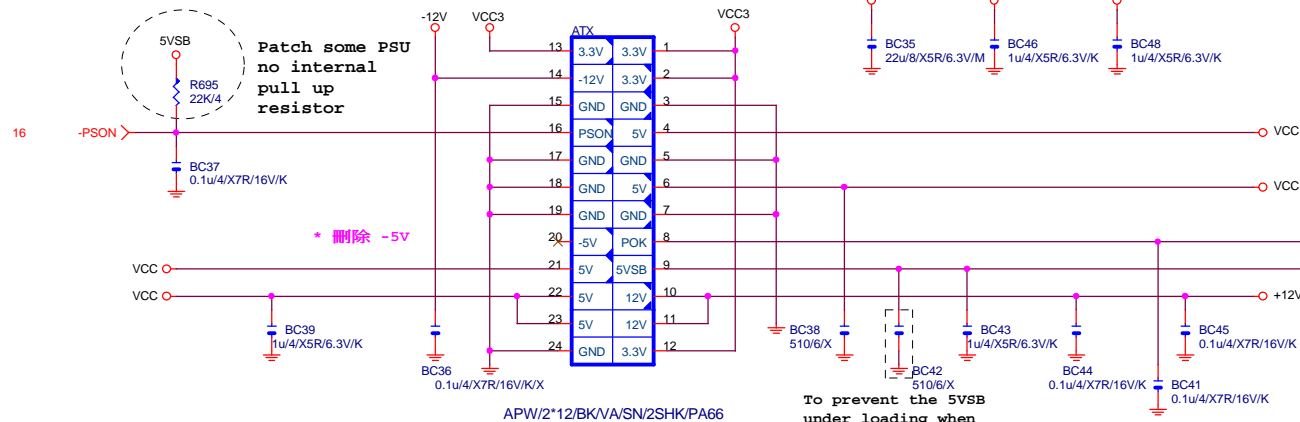
At least 10ms delay after
3VDUAL stabel

不上件

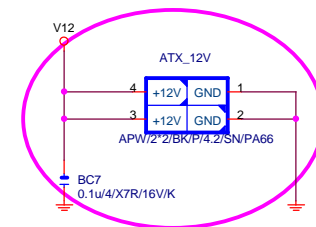
Gigabyte Technology

Title		
DISCRETE POWER		
Size	Document Number	Rev
Custom	GA-H110M-DS2	1.0
Date:	Monday, October 19, 2015	Sheet 29 of 46

ATXX24 POWER CONNECTOR

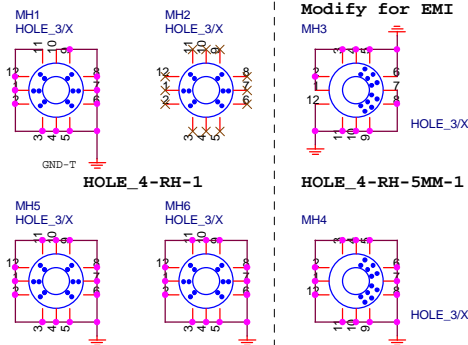


ATXX4 POWER CONNECTOR

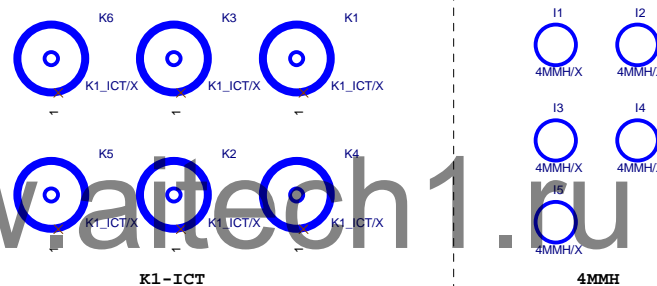


螺絲孔

MH1:GND-T
FOR EMI
TEST驗證

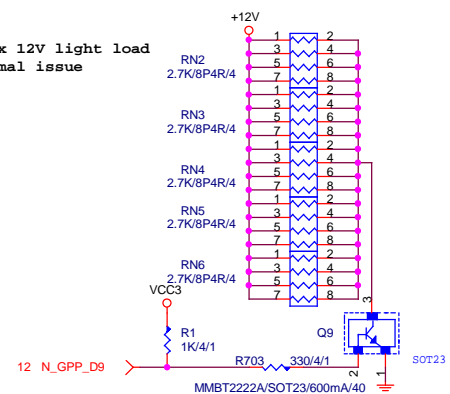


固定孔/光學點



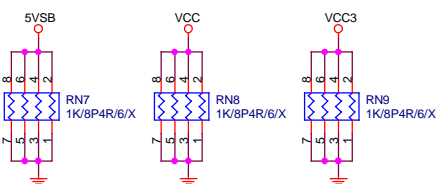
+12V DUMMY LOAD

To fix 12V light load abnormal issue



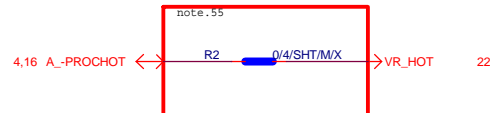
【技術通報R&D技術通報153】

DUMMY LOAD

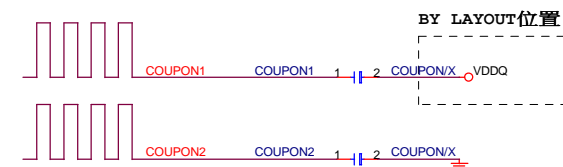


-PROHOT

* 保留 ?



COUPON



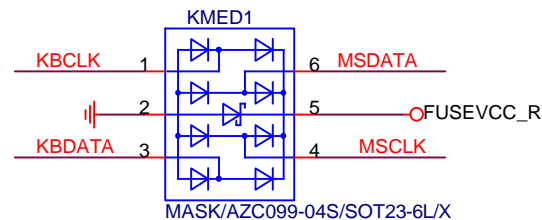
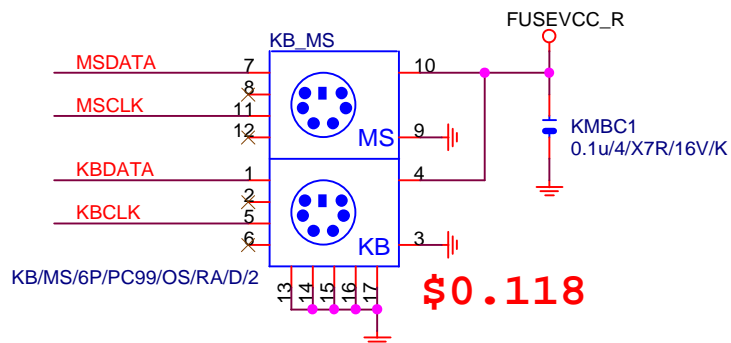
Gigabyte Technology

Title		
ATX POWER CONNECTOR		
Size	Document Number	Rev
Custom	GA-H110M-DS2	1.0
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KB_MS_USB

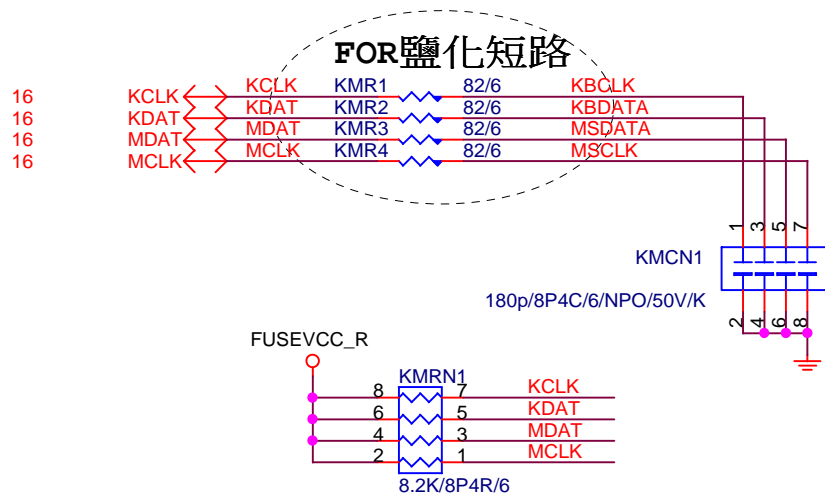
Rev: 0.7

ESD



KB_MS_USB DAMPING/PU

KB_MS_USB PWR



Gigabyte Technology

Title

KB_MS_USB

Size
A

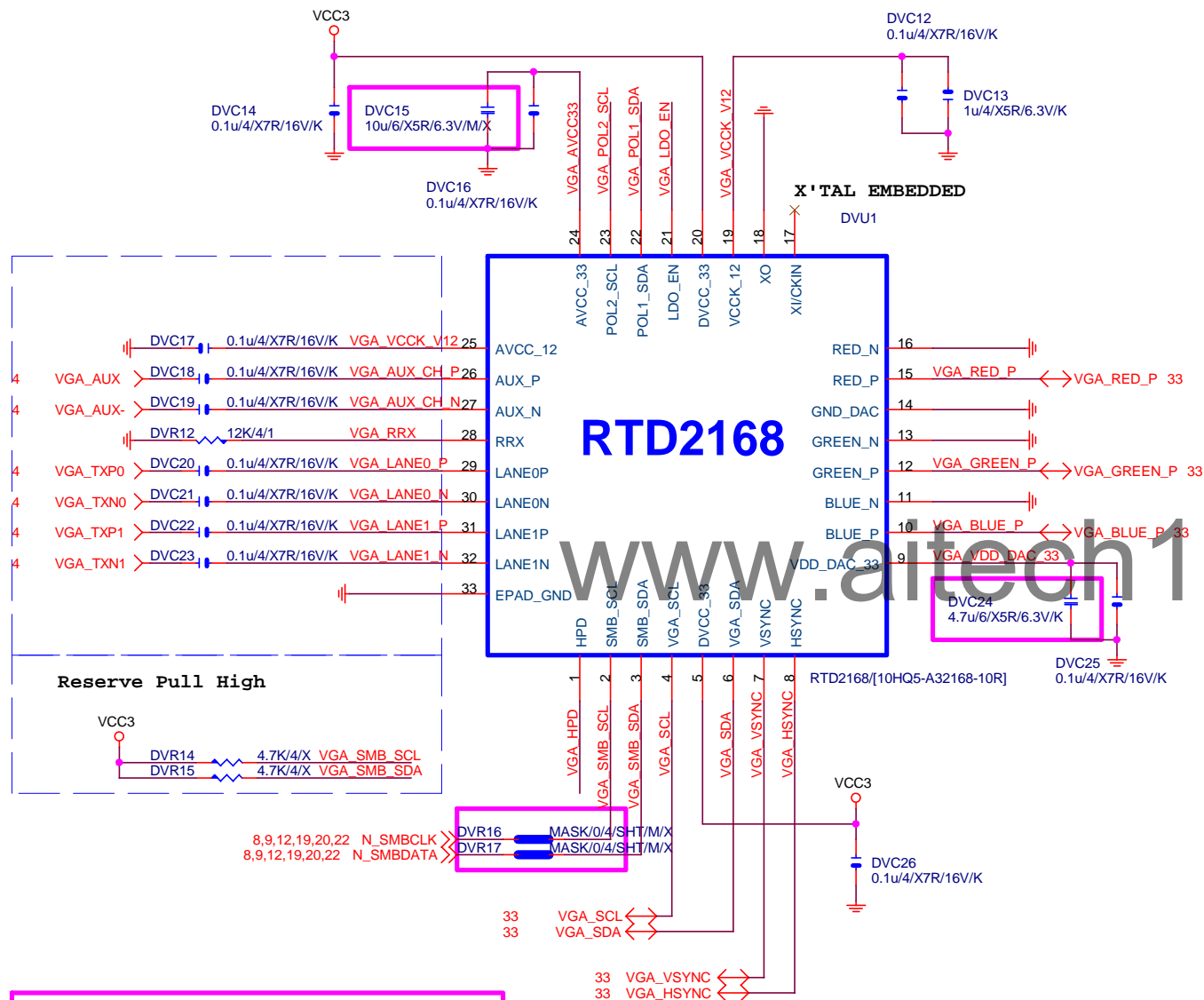
Document Number

GA-H110M-DS2

Rev
1.0

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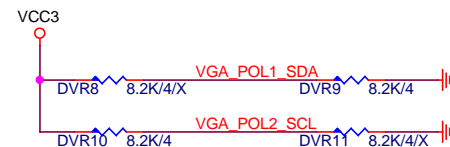
放置PCH端



POWER

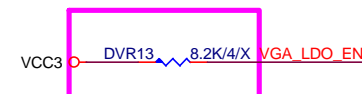


Power on latch



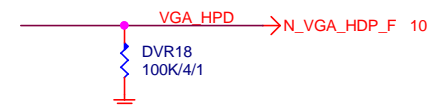
		POL1_SDA(PIN22)	
		0	1
POL2_SCL (PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

Embedded LDO

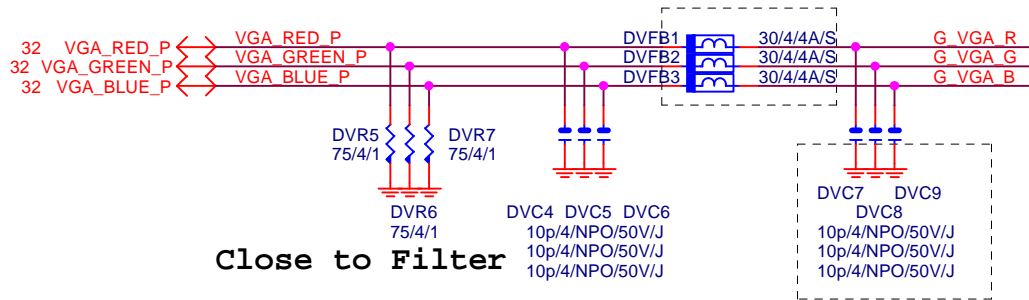
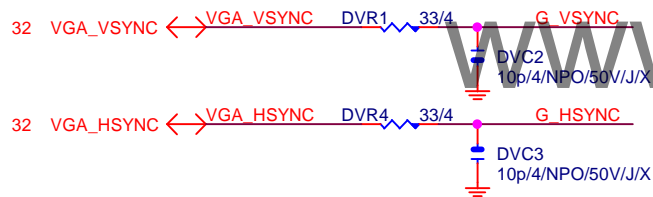
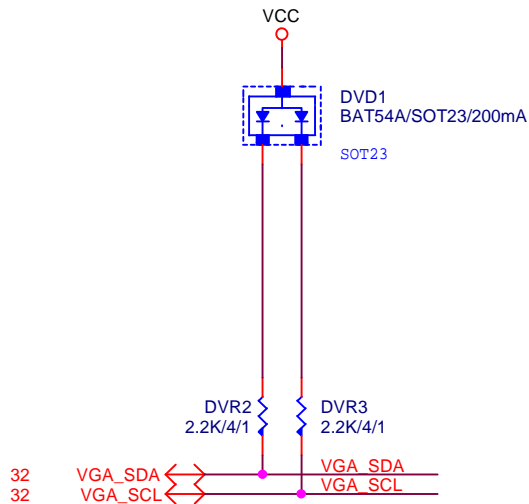


LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

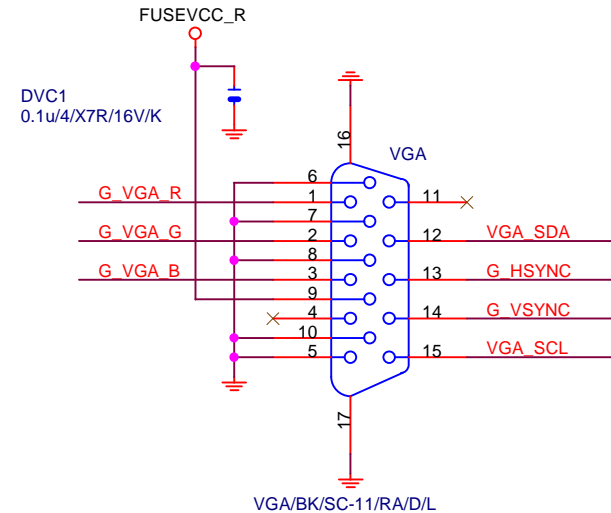
DP HPD



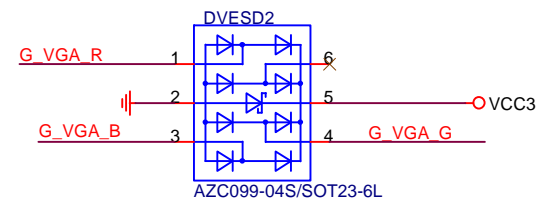
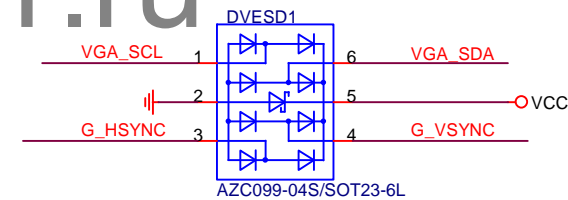
VGA SIGNAL R1.03



VGA CONN.



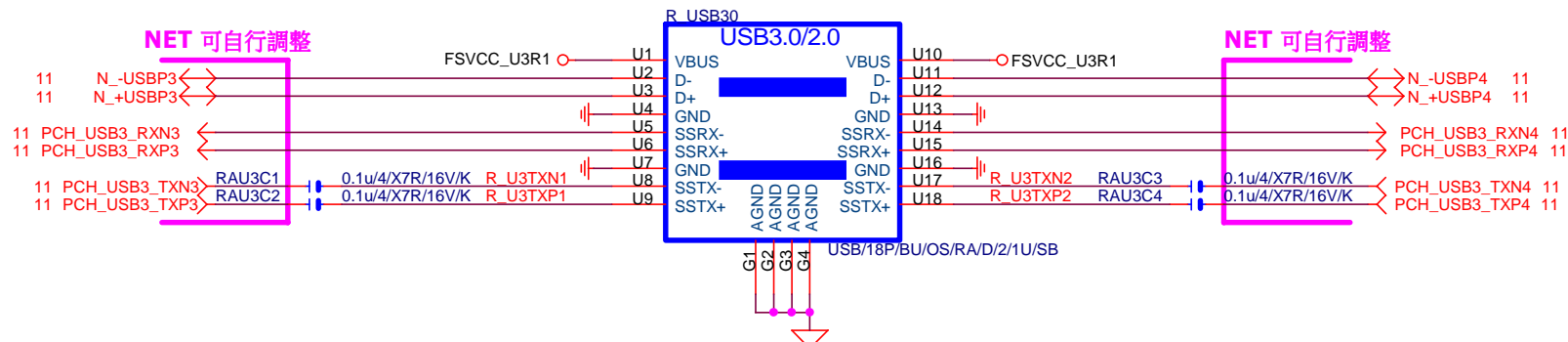
VGA ESD



Gigabyte Technology			
NXP-PTN3356			
Title	GA-H110M-DS2		
Size	Document Number	Rev	1.0
Custom			
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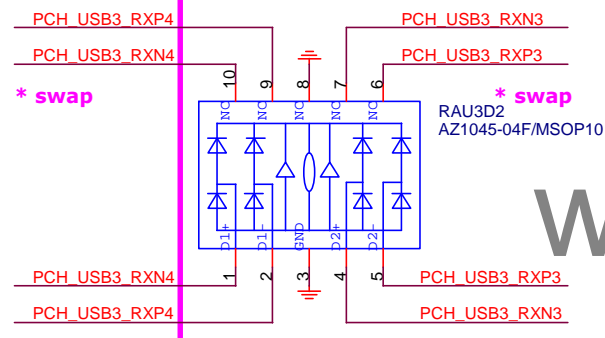
Rev: 0.7

ESD 可自行SWAP PIN ,CONN端 NET 名稱 不可

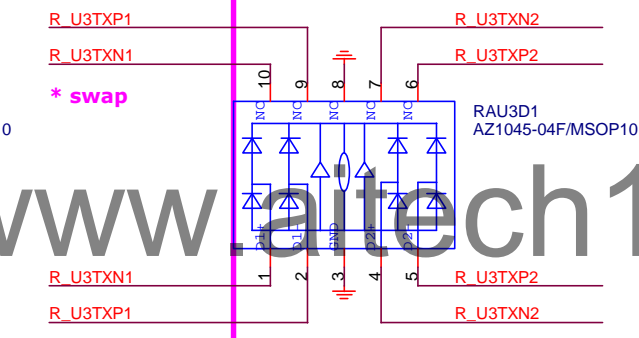


ESD

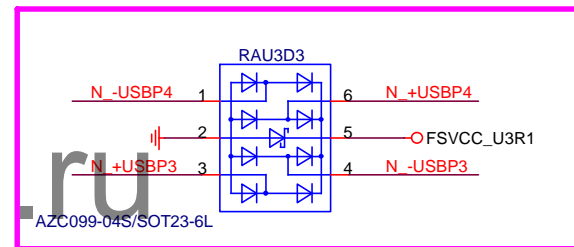
NET 可自行調整



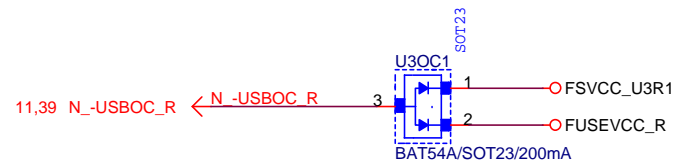
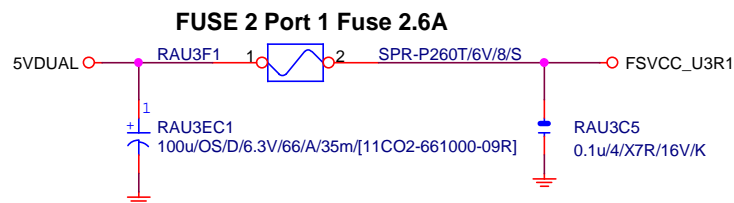
NET 可自行調整



NET 可自行調整

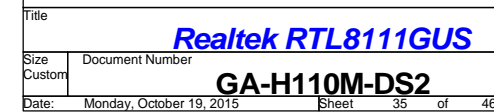


FUSE



Gigabyte Technology

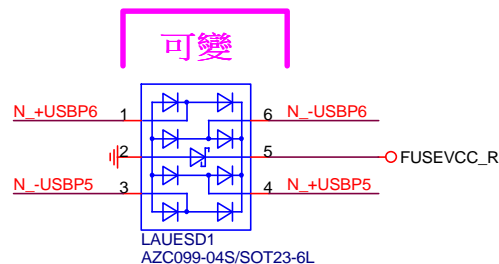
Title			R_USB30,USB_OC
Size			Document Number
Custom			GA-H110M-DS2
Date:			Monday, October 19, 2015
Sheet			34 of 46
Rev			1.0



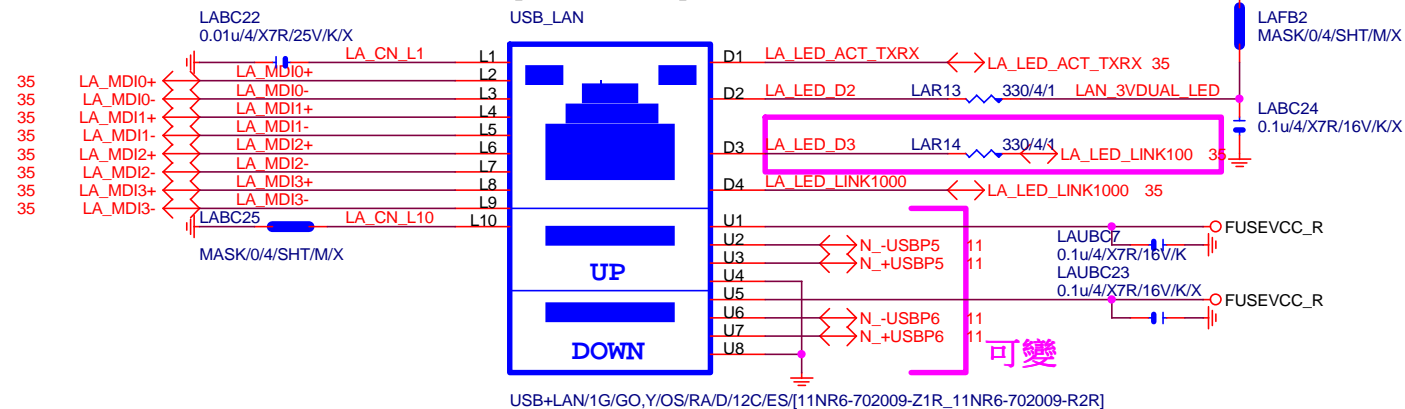
MDI ESD預留 *

R1.06

note:可變更USB NAME



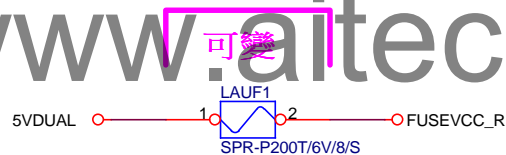
note:可變更USB NAME



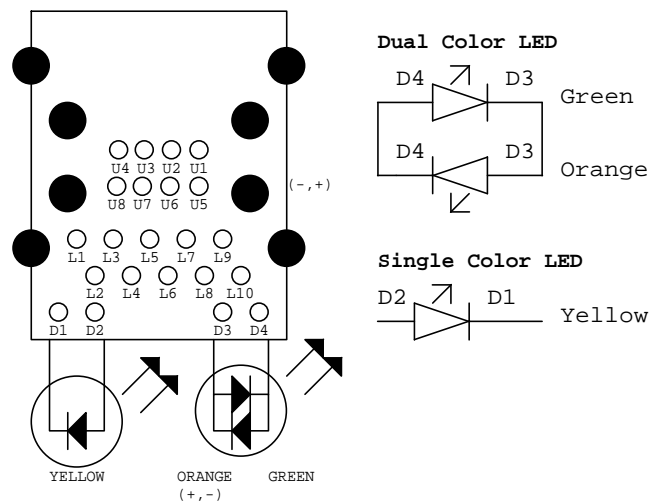
LA MDI-->100歐姆:[20/4/8/4/20]

USB POWER

note:可變更FUSE

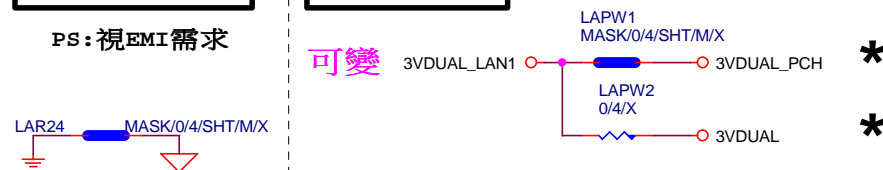


Close to connector
USB_LAN 2-Port 2.0A
FUSE-0805



LAN POWER

note: lan power連接及電流



Gigabyte Technology

LAN CONNECTOR-RTL8111G

Size	Document Number
Custom	

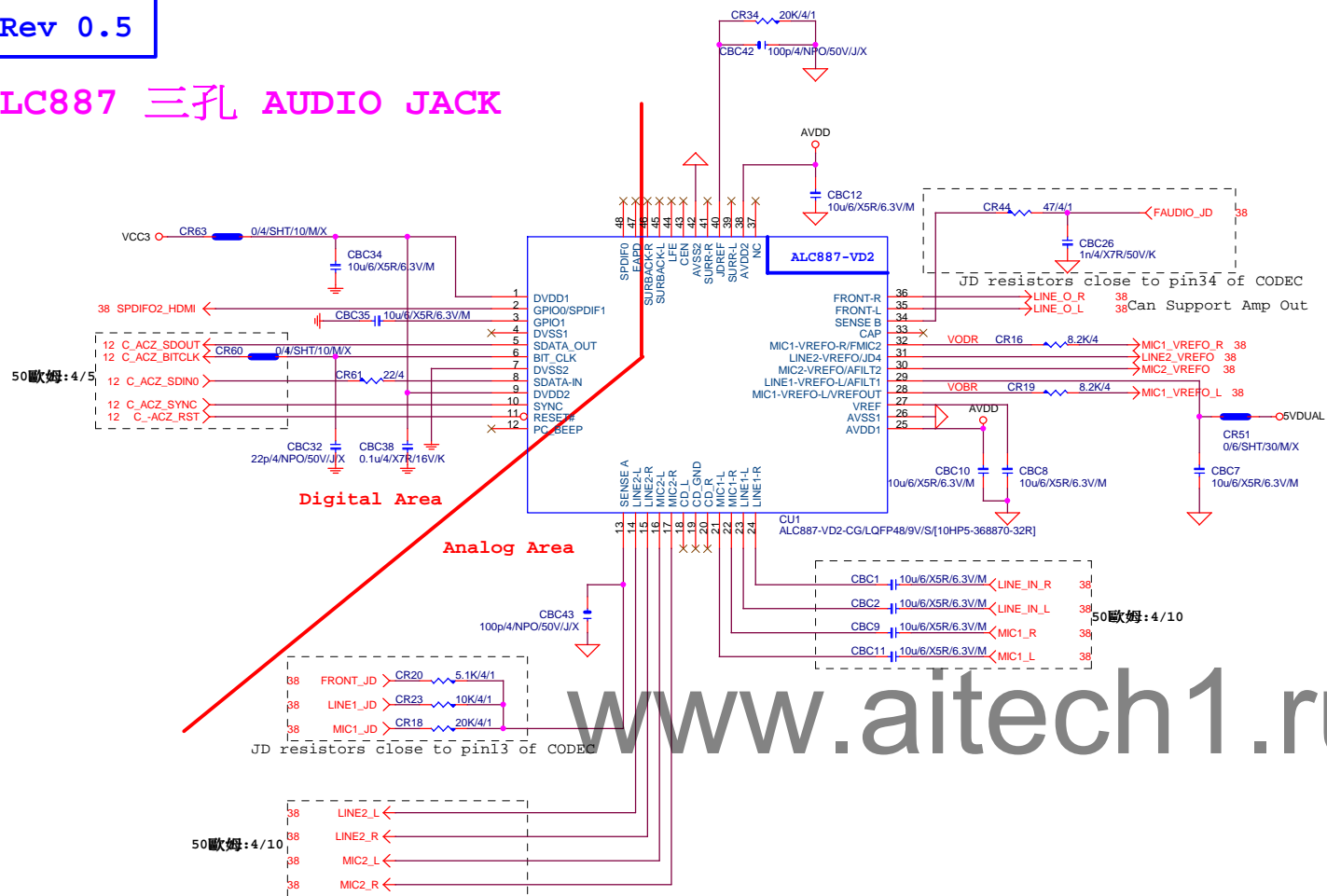
GA-H110M-DS2

Rev	1.0
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ALC887 三孔 AUDIO JACK

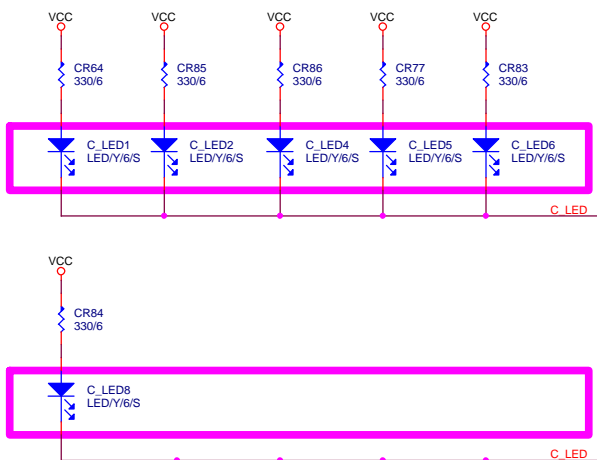


LAYOUT注意: 螺絲孔下GND方式

1. MH1空間夠, 下DGND
空間不夠, 改為Isolate
2. MH2一律改為Isolate

○ MH1	MH2 ○
DGND	Isolate

VALUE可變, LED顏色請自行修改
(預設: 低亮度黃色LED: LED/Y/6/S)



- BOM OPTION :
1. Chemicon音效電容
 2. 金屬外罩 Reserve (上件與否, 依照各Model spec)
 3. LED Reserve (上件與否和LED顏色, 依照各Model spec)

LAYOUT注意: 要加

GND切割線

音效區域印刷

Gigabyte Technology

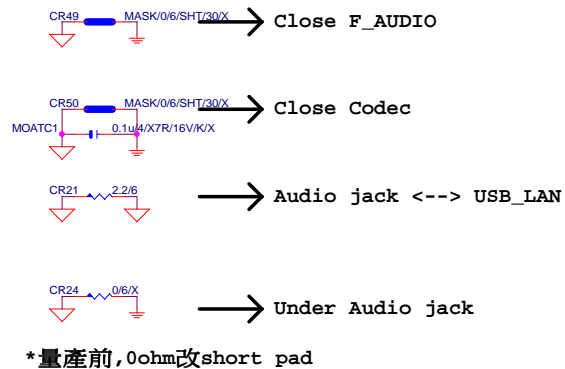
Title HD AUDIO ALC887

Size Custom Document Number GA-H110M-DS2

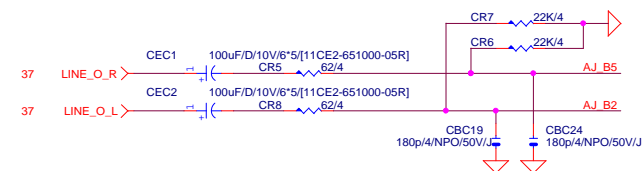
Rev 1.0

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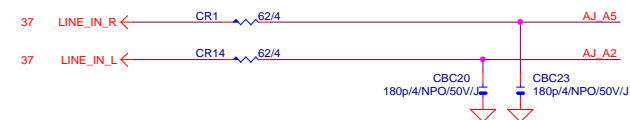
Rev 0.5



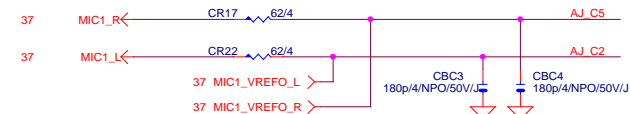
LINE-OUT



LINE-IN



MIC-IN

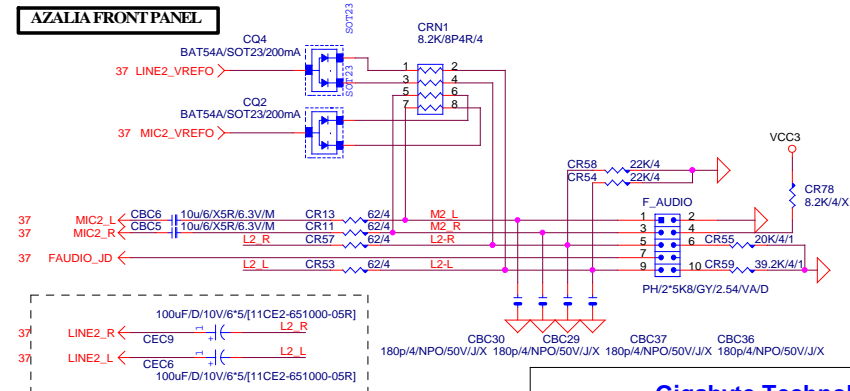


SURROUND

CEN/LFE

SURRBACK

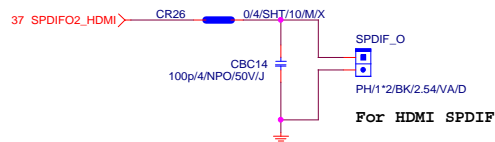
AZALIA FRONT PANEL



Gigabyte Technology

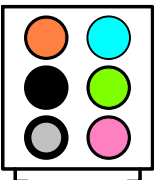
Title			
AUDIO JACK			
Size	Document Number	GA-H110M-DS2	
Custom			Rev 1.0
Date:	Monday, October 19, 2015	Sheet	38 of 46

SPDIF_OUT

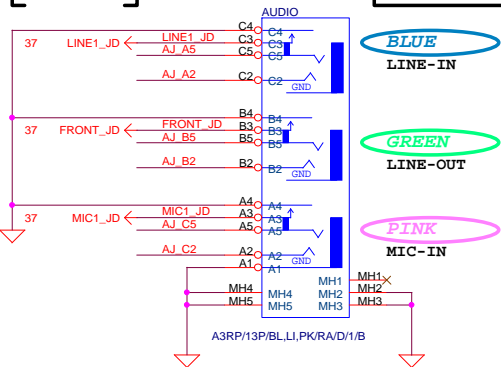


SPDIF_IN

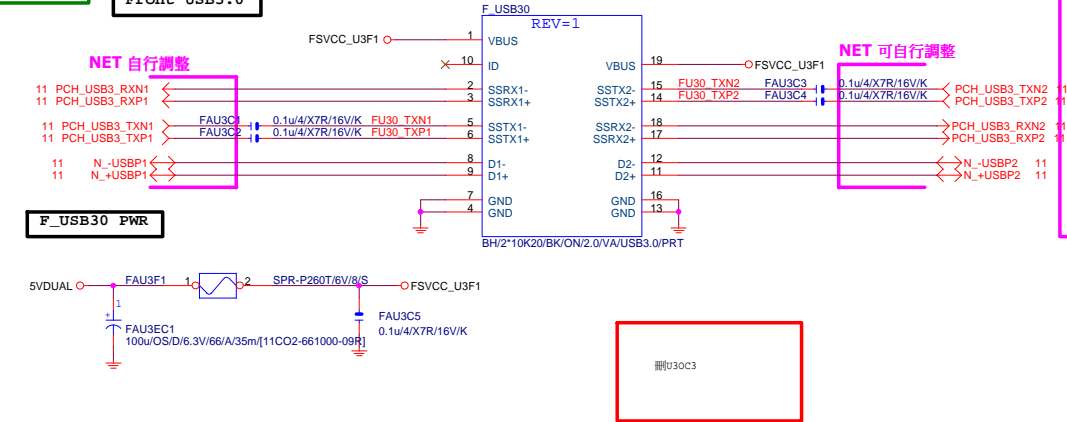
AZALIA JACK



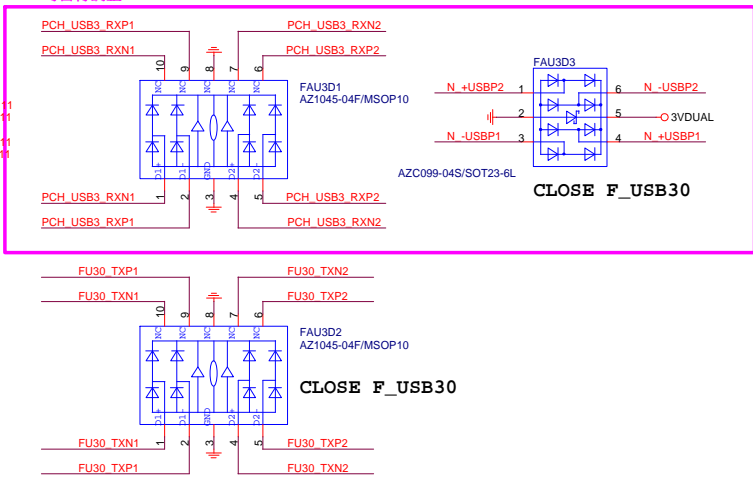
AZALIA JACK



Front USB3.0

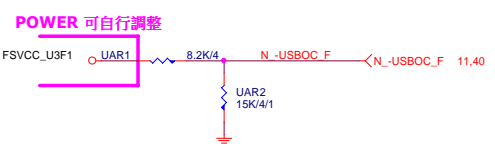


NET 可自行調整

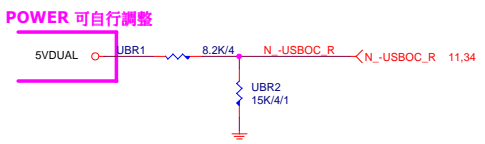


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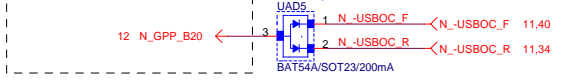
-USBOC_F



-USBOC_R



* 接 PCH N_GPP_B21
PCH PU 3vdual



Gigabyte Technology

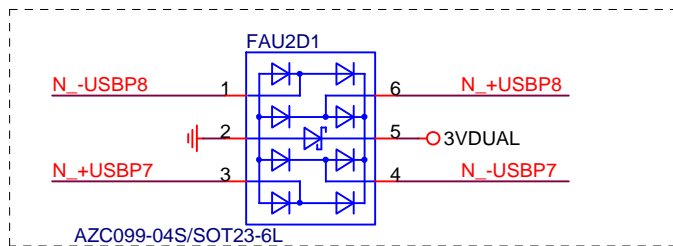
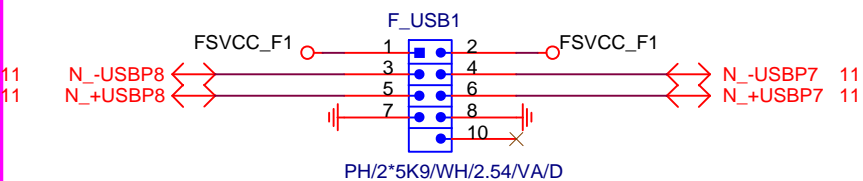
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R_USB30,F_USB30, USB_OC			
Size	Document Number	GA-H110M-DS2	
Custom		Rev 1.0	
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FRONT USB1

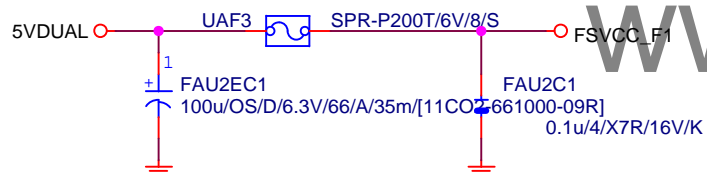
NET 可變

FUSB2X5-HS



Close to connector

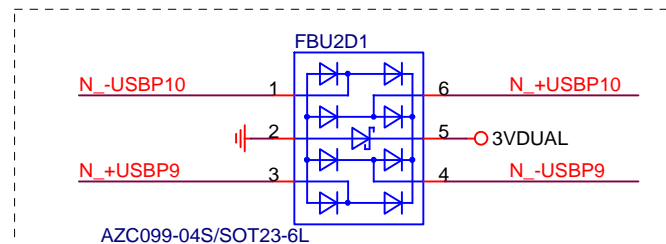
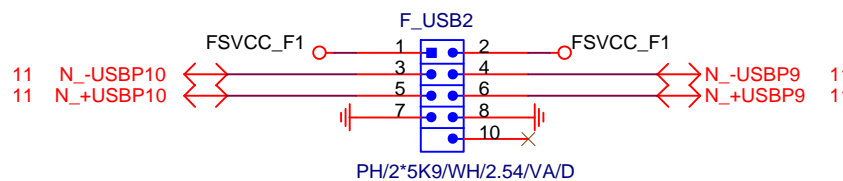
FUSE 2 Port 1 Fuse 2A



FRONT USB2

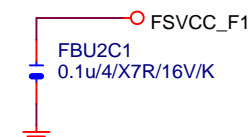
NET 可變

FUSB2X5-HS

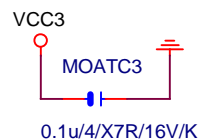
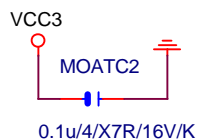
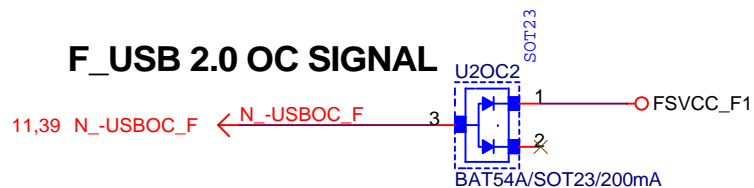


Close to connector

FUSE 2 Port 1 Fuse 2A



F_USB 2.0 OC SIGNAL



Gigabyte Technology

Title

USB2.0

Size
A

Document Number

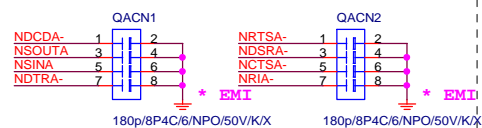
GA-H110M-DS2

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note.52

* 接 N_-PCIE_WAKE 12,16,19,20

NRIA- OAR1 75K/4/1/X

OAR2 8.2K/4/X

OAC1

MMBT2222A/SOT23/600mA/40/X SOT23

OABC1 0.1u/4/X7R/16V/K/X

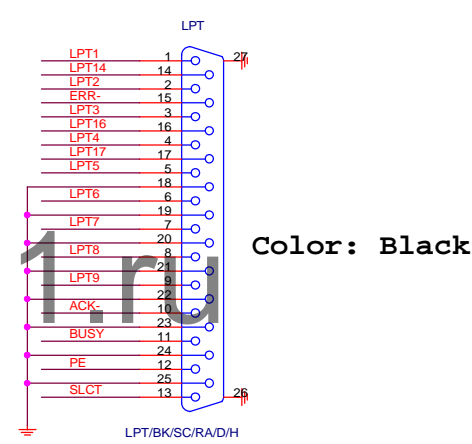
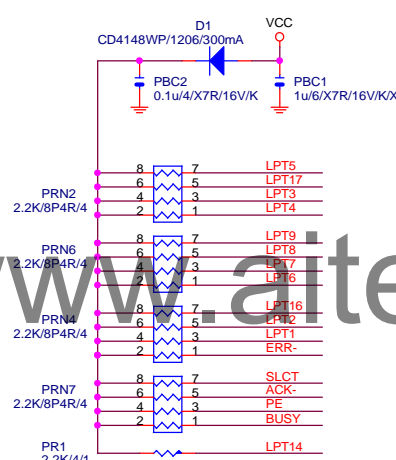
N_-PCIE_WAKE 12,16,19,20

Figure 10 shows the pin connections for the 68800. The diagram is organized into three main sections, each representing an 8-pin connector (PRN5, PRN3, and PRN1) and its corresponding connections to the 68800 and external devices.

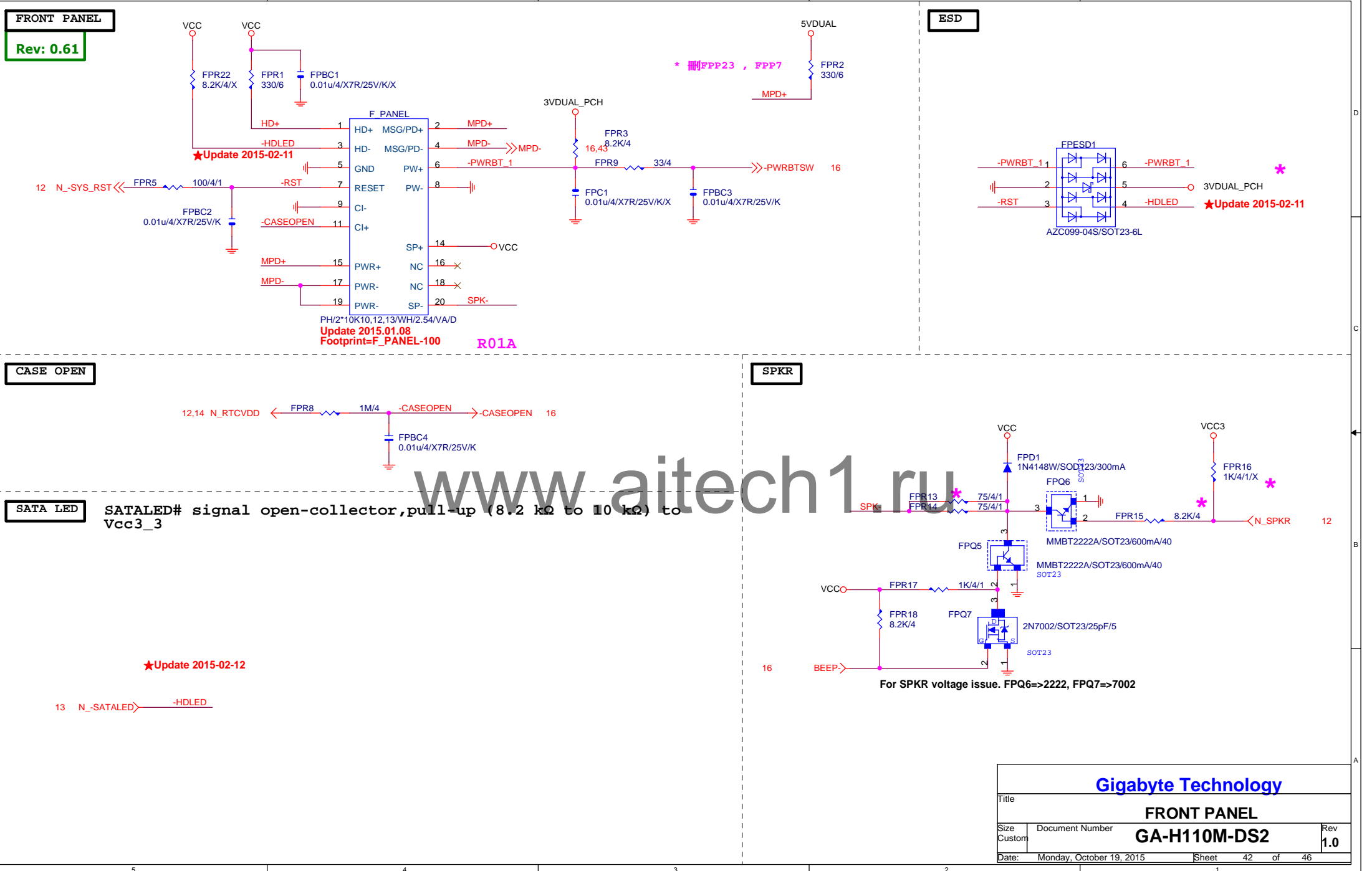
- PRN5 Connector:**
 - Left side (68800 pins): AFD (1), STB (2), PD0 (3), INIT (4), INIT- (5).
 - Right side (External devices): LPT14 (1), LPT1 (2), LPT2 (3), LPT16 (4).
- PRN3 Connector:**
 - Left side (68800 pins): PD2 (1), PD1 (2), SLIN (3), PD3 (4).
 - Right side (External devices): LPT4 (1), LPT3 (2), LPT17 (3), LPT5 (4).
- PRN1 Connector:**
 - Left side (68800 pins): PD4 (1), PD5 (2), PD6 (3), PD7 (4).
 - Right side (External devices): LPT6 (1), LPT7 (2), LPT8 (3), LPT9 (4).

Each connector section is labeled "68/8P4R/4" below it. Additionally, there are connections for error and control signals at the bottom:

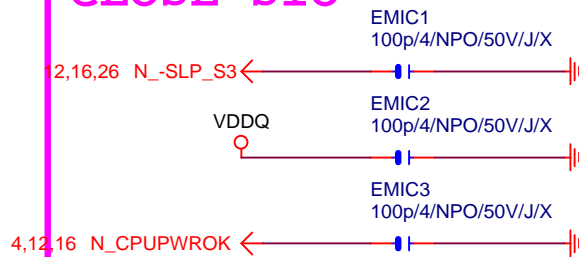
- Left side: ERR- (1), ACK- (2), BUSY (3), PE (4), SLCT (5), PDIO_7I (6).
- Right side: ERR- (1), ACK- (2), BUSY (3), PE (4), SLCT (5), PDIO_7I (6).



Thunderbolt (N/A)



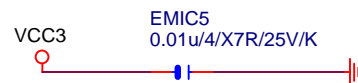
CLOSE SIO



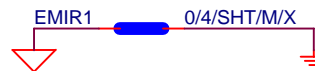
CLOSE PCH



close to PCH (NR17)



R_USB30_2 & DVI 之間



close to SIO (PIN92)MPD-

**GIGABYTE™**

Title

EMI/ESDSize
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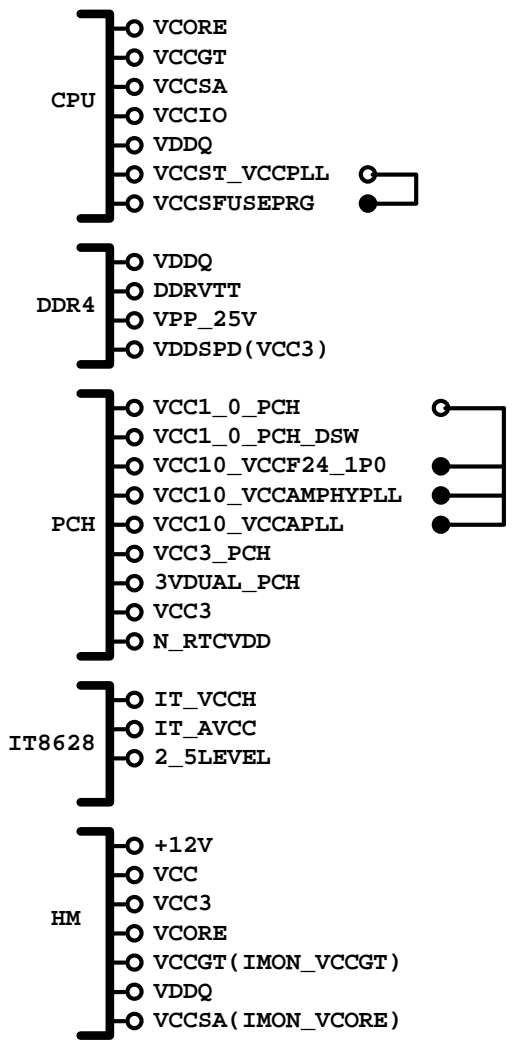
Rev

1.0

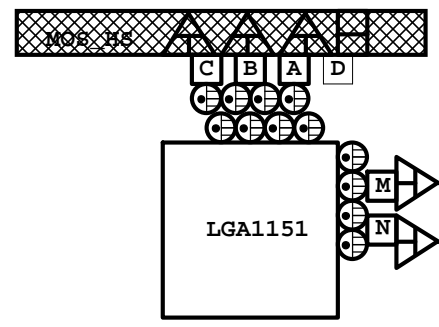
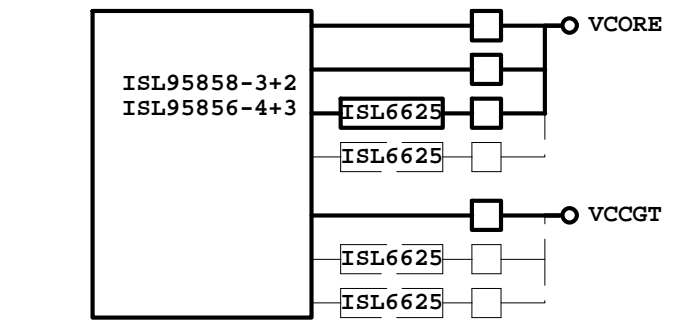
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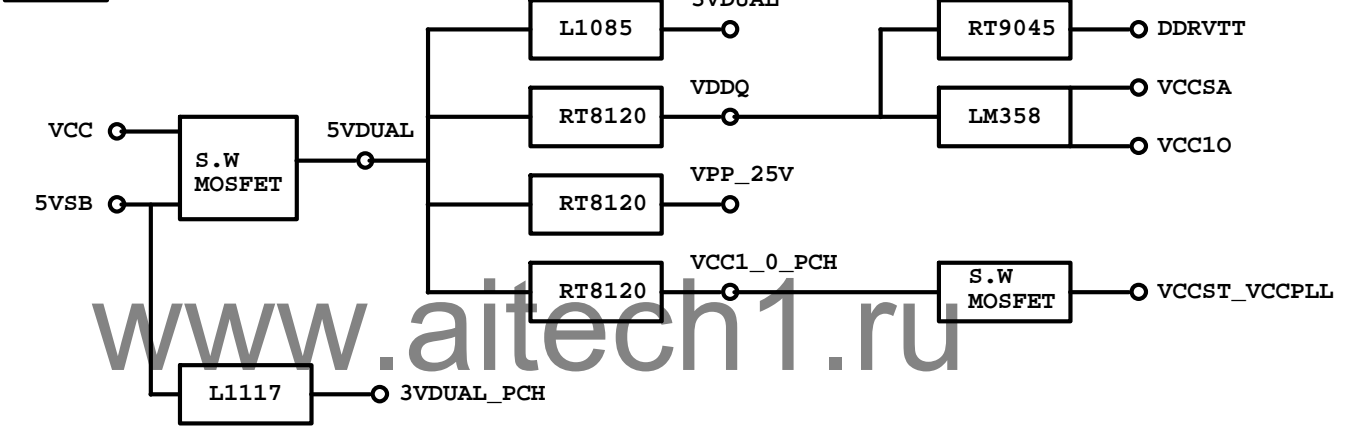
POWER BLOCK MAP



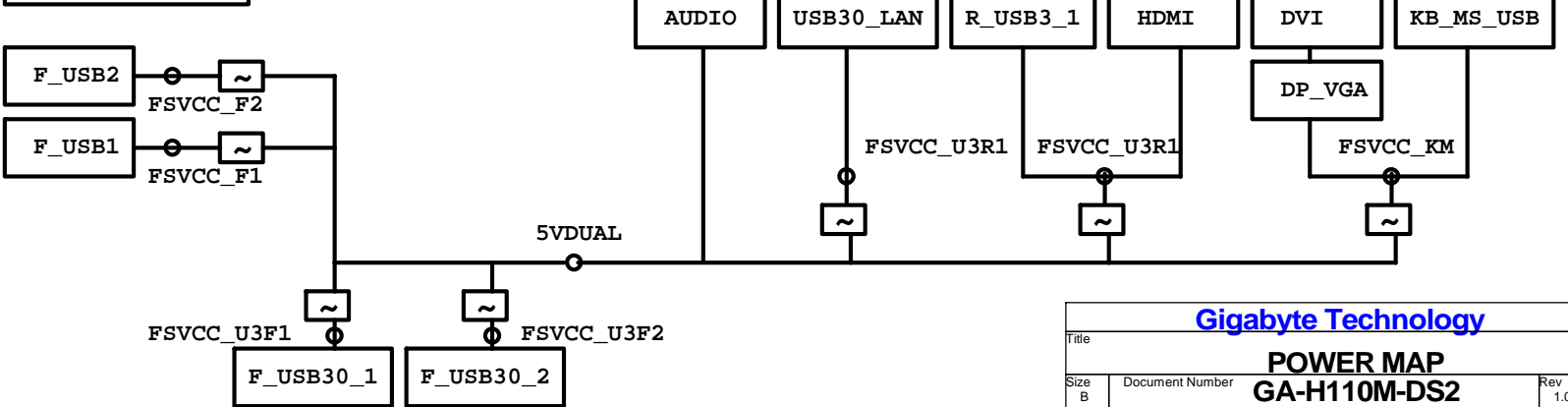
VCORE/VCCGT



POWER



FUSE POWER F/R



固態電容料號.請自行修改

日系黑色固態	Capture Value
11C02-C85600-01R	560u/FP/D/6.3V/68/C/8m
11C05-C82700-01R	270u/FP/D/16V/88/C/12m
11C05-C61000-01R	100u/OS/D/16V/66/C/30m
11C02-C51000-01R	100u/FP/D/6.3V/65/C/13m

日系一般固態	Capture Value
11C02-685600-01R	560u/FP/D/6.3V/68/8m
11C05-882700-01R	270u/FP/D/16V/88/12m
11C05-661000-03R	100u/OS/D/16V/66/30m
11C02-651000-02R	100u/OS/D/6.3V/66/30m

台系固態	Capture Value
11C02-661000-09R	100u/OS/D/6.3V/66/A/35m
11C05-691000-09R	100u/OS/D/16V/69/A/35m
11C05-8C2700-09R	270u/FP/D/16V/8C/A/10m
11C02-695600-09R	560u/FP/D/6.3V/69/A/11m

IRON CHOKE

	料號	Capture Value	SIZE	Footprint
DIP	11LC5-M4500C-01R	0.5uH/40A/IMD109/M/D	10*10	CHOKE05U-40A-1PQ-3
DIP	11LC5-M2500C-01R	0.5uH/20A/IMD0809/M/D	8*8	CHOKE1U-R50M-IF

Ferrite

	料號	Capture Value	SIZE	Footprint
DIP	11LC5-F3500C-11R	0.5uH/32A/INCG109/FSI/D	10*10	CHOKE05U-40A-1PQ-3
DIP	11LC5-F2500C-11R	0.5uH/25A/INC0809/F/D	8*8	CHOKE1U-R50M-IF
SMD	未建(SIUC1007-R30M-JJ1W)		10*7	CHOKE11X8MM-SMD

BEAD

	料號	Capture Value	SIZE	Footprint
DIP	10LFB-15470A-01R	47/4030/15A/S	4*3	BEADC8B-BPH_SMD

PWM料號

	料號	Capture Value	Footprint
PWM	ISL95856	10TA1-695856-01R	IC52QFN-6x6-G
PWM	ISL95858	10TA1-695858-01R	IC52QFN-6x6-G
PWM	IR35201	10TA1-635201-00R	IC56QFN-9VRS4339
PWM	IR3570	10TA1-603570-00R	IC40MLFP-ISL95835

GIGABYTE™

Title

RT8120_DDR4 POWER

Size Custom

Document Number

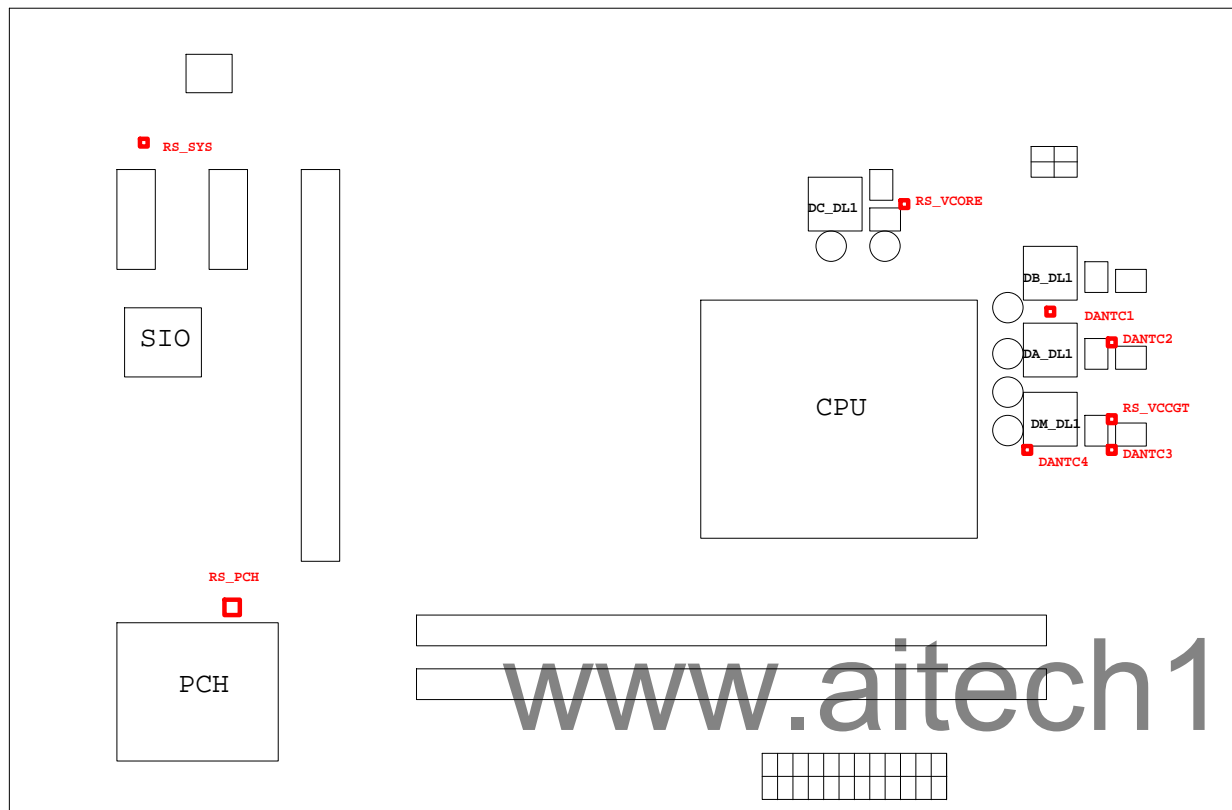
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熱敏電阻	擺放靠近位置	走線方式
DANTC4	DM_DL1	Differential
DANTC1	DA_DL1	Differential
DANTC3	DM_DQ1	Differential
DANTC2	DA_DQ1	Differential
RS_VCORE	DA_DQ1	N/A
RS_VCCGT	DM_DQ1	N/A
RS_PCH	PCH	N/A
RS_SYS	CU1	N/A